



MB25
TFT TV
SERVICE MANUAL

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1. INTRODUCTION

17MB25 mainboard is based on MSTAR concept IC. This IC is capable of handling audio processing, video processing, scaling-display processing, 3D comb filter, OSD and text processing, 8 bit dual LVDS transmitter.

TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system is able to supply 2x10W (10%THD) audio output power for stereo speakers. Supported peripherals are:

The analog part of the board can support DVD module which is connected to mainboard through a cable.

The USB feature is supported through digital part of the mainboard.

- 1 RF input VHF1, VHF3, UHF @ 75Ohm(Common)
- 1 Side AV (SVHS, CVBS, HP, R/L_Audio) (Common)
- 1 SCART socket(Common)
- 1 YPbPr (Common)
- 1 PC input(Optional)
- 2 HDMI (Common)
- 1 Stereo audio input for PC(Common)
- 1 Line out(Common)
- 1 S/PDIF output(Common)
- 1 Side S-Video(Optional)
- 1 Headphone(Common)
- 1 Common interface(Optional)
- 1 Digital USB(Optional)
- 1 RS232(Optional)

2. TUNER

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

1.1 General description of TDTC-G101D:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

1.2 Features of TDTC-G101D:

- Digital Half-NIM tuner for COFDM
- Covers 3 Bands(From 48MHz to 862MHz for COFDM,
- From 45.25MHz to 863.25MHz for CCIR CH)

- Including IF AGC with SAW Filter
- Bandwidth Switching (7/8 MHz) possible
- DC/DC Converter built in for Tuning Voltage
- Internal(or External) RF AGC, Antenna Power Optional

1.3 Pin Configuration

PIN NAME	PIN No.	PIN Description
Ant PWR	1	+5V (for Active Antenna), Optional
B1	2	+ 5V (for Loop through & DC-DC)
RF AGC	3	N.C
SCL	4	I ² C Bus for TUNER PLL
SDA	5	I ² C Bus for TUNER PLL
B2	6	+ 5V (for TU & IF AGC AMP)
Vtu T.P	7	N.C
AS	8	PLL IC Address selection
IF AGC Control	9	IF AGC Control
DIF2	10	Total IF Output2
DIF1	11	Total IF Output1
AIF	12	Tuner IF Output

3. AUDIO AMPLIFIER STAGE WITH TPA3101

3.1 General Description of TPA3101

The TPA3101D2 Rev.A evaluation module consists of a single 10-W, class-D, stereo audio power amplifier complete with a small number of external components mounted on a circuit board that can be used to directly drive a speaker with an external analog audio source as the input.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36dB.

The outputs are fully protected against shorts to GND, Vcc and output to output shorts with an auto recovery feature and monitor output.

3.2 Features of TPA3101

- 10-W/ch into an 8-Ω Load From a 13-V Supply
- 9.2-W/ch into an 8-Ω Load From a 12-V Supply
- Operates from 10 V to 26 V
- 87% Efficient Class-D Operation Eliminates
- Need for Heat Sinks
- Four Selectable, Fixed Gain Settings

- Differential Inputs
- Thermal and Short-Circuit Protection With
- Auto Recovery Feature
- Clock Output for Synchronization With Multiple Class-D Devices
- Surface Mount 7 mm ´ 7 mm, 48-pin QFN Package
- Surface Mount 7 mm ´ 7 mm, 48-pin HTQFP Package

3.3 Pin Configuration of TPA3101

TERMINAL			I/O	DESCRIPTION
NAME	QFN NO.	HTQFP NO.		
SHUTDOWN	44	44	I	Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.
RINN	2	2	I	Negative audio input for right channel. Biased at VREG/2.
RINP	3	3	I	Positive audio input for right channel. Biased at VREG/2.
LINN	6	6	I	Negative audio input for left channel. Biased at VREG/2.
LINP	5	5	I	Positive audio input for left channel. Biased at VREG/2.
GAIN0	8	7, 8	I	Gain select least significant bit. TTL logic levels with compliance to VREG.
GAIN1	9	9	I	Gain select most significant bit. TTL logic levels with compliance to VREG.
GND		1, 12, 13, 24, 25, 36, 37		Connect to the thermal pad.
MUTE	45	45	I	Mute signal for quick disable/enable of outputs (HIGH = outputs high-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
FAULT	46	46	O	TTL compatible output. HIGH = short-circuit fault. LOW = no fault. Only reports short-circuit faults. Thermal faults are not reported on this terminal.
BSLP	18	18	I/O	Bootstrap I/O for left channel, positive high-side FET.
PVCCCL	26, 27	26, 27		Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
LOUTP	19, 20	19, 20	O	Class-D 1/2-H-bridge positive output for left channel.
PGNDL	28, 29	28, 29		Power ground for left channel H-bridge.
LOUTN	21, 22	21, 22	O	Class-D 1/2-H-bridge negative output for left channel.
BSLN	23	23	I/O	Bootstrap I/O for left channel, negative high-side FET.
VCLAMPL	30	30		Internally generated voltage supply for left channel bootstrap capacitor.
VCLAMPR	31	31		Internally generated voltage supply for right channel bootstrap capacitor.
BSRN	38	38	I/O	Bootstrap I/O for right channel, negative high-side FET.
ROUTN	39, 40	39, 40	O	Class-D 1/2-H-bridge negative output for right channel.
PGNDR	32, 33	32, 33		Power ground for right channel H-bridge.
ROUTP	41, 42	41, 42	O	Class-D 1/2-H-bridge positive output for right channel.
PVCCR	34, 35	34, 35		Power supply for right channel H-bridge, not connected to PVCCCL or AVCC.
BSRP	43	43	I/O	Bootstrap I/O for right channel, positive high-side FET.
AGND	4, 17	4, 17		Analog ground for digital/analog cells in core.
ROSC	14	14	I/O	I/O for current setting resistor of ramp generator.
MSTR/SLV	10	10	I	Master/Slave select for determining direction of SYNC terminal. HIGH=Master mode, SYNC terminal is an output; LOW = slave mode, SYNC terminal accepts a clock input. TTL logic levels with compliance to VREG.
SYNC	11	11	I/O	Clock input/output for synchronizing multiple class-D devices. Direction determined by MSTR/SLV terminal. Input signal not to exceed VREG.
VBYP	16	16	O	Reference for preamplifier. Nominally equal to 1.25 V. Also controls start-up time via external capacitor sizing.
VREG	15	15	O	4-V regulated output for use by internal cells, GAINx, MUTE, and MSTR/SLV pins only. Not specified for driving other external circuitry.
AVCC	48	47, 48		High-voltage analog power supply. Not internally connected to PVCCR or PVCCCL.
NC	1, 7, 12, 13, 24, 25, 36, 37, 47			Not internally connected.
Thermal Pad	-	-	-	Connect to AGND and PGND – should be star point for both grounds. Internal resistive connection to AGND and PGND. Thermal vias on the PCB should connect this pad to a large copper area on an internal or bottom layer for the best thermal performance. <i>The Thermal Pad must be soldered to the PCB for mechanical reliability.</i>

4. MICROCONTROLLER (MSTAR)

4.1 General Description

The MST6WB7GQ-3 is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, two video de-interlacers, two scaling engines, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6WB7GQ-3 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

4.2 Features

LCD TV controller with PIP/POP display functions

- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- Full function PIP/PBP/POP
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controller engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 296-pin LQFP

NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- Motion adaptive 3-D comb filter for NTSC/PAL
- 8 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- Macrovision detection
- CVBS video output

Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

Multi-Standard TV Sound Decoder

- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx4, mono, and SIF audio inputs
- L/Rx3 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, and virtual stereo/surround
- Optional advanced surround available (Dolby1, SRS2, BBE3... etc)

Digital Audio Interface

- I2S digital audio input & output
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Three analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

DVI/HDCP/HDMI Compliant Input Port

- Two HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection(HDCP) 1.1 compliant receiver

5. INTEGRATED DVB-T RECEIVER (CHEERTEK)

5.1 General Description

CT216T is a highly integrated single chip for DVB-T compliant STB solution. Compared with Cheertek's previous generations of STB receiver devices. CT216T further integrates COFDM demodulator USB 2.0 HS host controller, memory card reader, 1/2-bit SPIFlash interface, audio DAC, PWM in/out and SAR-ADC functions. In addition special enhancements are provided such as MPEG-4 video decoding, 16-bit OSD with anti-flickering,

HW JPEG decoding, flesh tone and black-white extensions, and improvement of small video quality.

CT216T includes COFDM demodulator transport stream de-multiplexer, DVB-CSA compliant de-scrambler, RISC MPUs, MPEG-1/2/4 AV decoder, digital TV encoder, audio DACs, USB 2.0 HS host controller, memory card reader, smart card reader, CI controller and other peripherals.

Cli216T is designed in focus on the market of single tuner input product which makes, it a cost effective solution. Supports include free to air, conditional access for SC (Smart card) and CI portable devices, PVR, LCD TV, and other DVB-T applications.

5.2 Features

COFDM Demodulator

- ETSI EN 300 744 DVB-T NorDig Unified 1.0.3, and D-book compliant
- Automatic spectral inversion, detection
- Integrated ADC
- Direct IF (36.167 MHz or 43.75 MHz) or low IF (4.57 MHz) supported
- Single IF AGC or dual RF/IF AGC controls with $\Delta\Sigma$ modulation
- Impulsive noise cancellation
- Carrier acquisition range: ± 400 kHz (extensible to ± 600 kHz in 8MHz BW)
- Adjacent channel interference (ACI) filter, for supporting 6, 7, and 8MHz channels with one 8MHz analog filter
- Co-channel interference (CCI) suppression
- RF signal strength monitor

MPU

- Three 32-bit RISC MPU run up to 166MHz with total 448DMIPS
- 8KB I-Cache and 8KB D-Cache
- Two general purpose timers
- Watchdog timer
- DSU for source level debug

Memory

- 6-bit SDRAM controller supports up to 32MB (16MB for 128-pin)
- Unified memory architecture
- Parallel flash (216-pin only)
- 1/2-bit SPI flash

Transport De-multiplexing

- TS, PES, and ES demultiplexing
- OneTS path
- CI CAM interface (216-pin only)
- 32 general purpose PID filters
- 32 Section filters
- CRC-32 accelerator
- DVB-CSA de-scramblers

Video Decoding and Processing

- MPEG-2 MP@ML
- MPEG-4 SP&ASP
- PAL/NTSC format conversion
- 3:2 pull down
- Zoom in/out from 1/16X to 16X
- HW JPEG decode
- 4/8/16-bit OSD with anti-flickering
- On chip NTSC/PAL TV encoder
- CVBS, S-VHS, and component video
- VBI insertion for Teletext, CC and WSS
- ITU-R BT.601 and ITU-R BT.656 outputs
- Flesh tone extension
- Black/white extension,

Audio Decoding and Processing

- MPEG-1: layer 1/2/3
- MPEG-2: layer 1/2
- Decode MPEG-2 and MPEG-1 audio at sampling frequency of 16K, 22.05K, 24K, 32K, 44.1K, and 48KHz
- Decode CU-DA at sampling frequency of 44.1 KHz
- SPDIF out for AC-3 by-pass
- Embedded 2 channels audio DAC for L/R outputs
- Digital mute control and volume adjustment

OSD(On Screen Display)

- There are total 9 display planes: border; background. video. RS1 (Rectangle Strip 1), RS2, OSD, RS3, RS4, and cursor.
- 4/8/16-bit OSD with anti-flickering and anti-flutter
- Support alpha-blending per color
- Adjustable brightness control in window
- Bitmap OSD
- Support horizontal pixel duplication to enlarge bitmap automatically
- Support sub-region redraw to facilitate bitmap display.

Digital TV Encoder

- NTSC-M, PAL-B, D, G, H, I, Nc, M encoding
- Four video DACs to provide 6 configuration output: modes
- Support CVBS, S-VHS. and component video outs
- VBI insertion for Teletext, CC and WSS
- Color burst amplitude control
- Programmable sync. level
- On chip, color-bar generator

High Speed I/O

- USB 2.0 HS host controller

- Memory card reader with SD, MMC, and MS interfaces
- Compliant with SD spec. 1.1 and MMC spec. 4.0 with 1-bit & 4-bit modes.
- Compliant with Memory Stick Pro format spec. 1.02 and Memory stick format spec 1.43 with 1-bit and 4-bit modes.

Peripherals

- Up to 3 full duplex UART with 16-byte FIFO
- 2-wire serial (2WS) in master mode . . .
- Up to 2 IS0-7816 compliant SC (1 in 128-pin, can also be used as UART)
- 5 digits 7-Segment LED control
- 5x3 two-dimension key scan
- 2 SAR-ADC input
- 4 PWM input/output
- 1 HW IR command decode
- GPIO

Electrical and Physical Characteristics

- Capable of using single 27MHz clock input crystal
- 1.8V and 3.3V dual power supply
- Power standby mode
- PQFP-128 (CT216T-Z) or LQFP-216 (CT216T-R) package

6. 4MX16 BIT SYNCHRONOUS DRAM (SDRAM)

6.1 General Description

The EM638165 SDRAM is a high-speed CMOS synchronous DRAM containing 64 Mbits. It is internally configured as 4 Banks of 1M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM638165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

6.2 Features

- Fast access time from clock: 4.5/5/5.4 ns
- Fast clock rate: 200/166/143 MHz
- Fully synchronous operation
- Internal pipelined architecture
- 1M word x 16-bit x 4-bank
- Programmable Mode registers

- CAS Latency: 2, or 3
- Burst Length: 1, 2, 4, 8, or full page
- Burst Type: interleaved or linear burst
- Burst stop function
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms
- CKE power down mode
- Single +3.3V ± 0.3V power supply
- Interface: LVTTL
- 54-pin 400 mil plastic TSOP II package
- Pb free and Halogen free
- 60-ball 6.4mm x 10.1mm VFBGA package
- Pb free

6.3 Pin Configuration

Symbol	Type	Description															
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.															
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.															
BA0,BA1	Input	Bank Activate: BA0, BA1 input select the bank for operation.															
		<table border="1"> <thead> <tr> <th>BA1</th> <th>BA0</th> <th>Select Bank</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>BANK #A</td> </tr> <tr> <td>0</td> <td>1</td> <td>BANK #B</td> </tr> <tr> <td>1</td> <td>0</td> <td>BANK #C</td> </tr> <tr> <td>1</td> <td>1</td> <td>BANK #D</td> </tr> </tbody> </table>	BA1	BA0	Select Bank	0	0	BANK #A	0	1	BANK #B	1	0	BANK #C	1	1	BANK #D
		BA1	BA0	Select Bank													
		0	0	BANK #A													
		0	1	BANK #B													
1	0	BANK #C															
1	1	BANK #D															
A0-A11	Input	Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 2M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.															
CS#	Input	Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.															
RAS#	Input	Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.															
CAS#	Input	Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."															
WE#	Input	Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.															

LDQM, UDQM	Input	Data Input/Output Mask: Controls output buffers in read mode and masks Input data in write mode.
DQ0-DQ15	Input / Output	Data I/O: The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are maskable during Reads and Writes.
NC/RFU	-	No Connect: These pins should be left unconnected.
V _{DDQ}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity. (3.3V ± 0.3V)
V _{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity. (0 V)
V _{DD}	Supply	Power Supply: +3.3V ± 0.3V
V _{SS}	Supply	Ground

7. 512K CMOS SERIAL FLASH – MX25L512

7.1 General Description

The MX25L512 is a CMOS 524,288 bit serial Flash memory, which is configured as 65,536 x 8 internally. The MX25L512 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input. The MX25L512 provide sequential read operation on whole chip. After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector (4K-bytes). To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current. The MX25L512 utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

7.2 Features

General

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 524,288 x 1 bit structure
- 16 Equal Sectors with 4K byte each
- Any Sector can be erased individually
- Single Power Supply Operation
- 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to V_{CC} +1V
- Low V_{CC} write inhibit is from 1.5V to 2.5V

Performance

- High Performance
- Fast access time: 85MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
- Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
- Fast erase time: 60ms(typ.) and 120ms(max.)/sector (4K-byte per sector) ; 1s(typ.) and 2s(max.)/chip(512Kb)
- Low Power Consumption
- Low active read current: 12mA(max.) at 85MHz, 8mA(max.) at 66MHz and 4mA(max.) at 33MHz
- Low active programming current: 15mA (max.)
- Low active erase current: 15mA (max.)
- Low standby current: 10uA (max.)
- Deep power-down mode 1uA (typical)
- Minimum 100,000 erase/program cycles

Software Features

- Input Data Format
- 1-byte Command code
- Block Lock protection
- The BP0~BP1 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
- JEDEC 2-byte Device ID
- RES command, 1-byte Device ID

Hardware Features

- SCLK Input
- Serial clock input
- SI Input
- Serial Data Input
- SO Output
- Serial Data Output
- WP# pin
- Hardware write protection
- HOLD# pin pause the chip without deselected the chip
- PACKAGE
- 8-pin SOP (150mil)
- All Pb-free devices are RoHS Compliant

8. 16MX16 BIT SYNCHRONOUS DRAM (SDRAM)

8.1 General Description

The EM63A165 SDRAM is a high-speed CMOS synchronous DRAM containing 256 Mbits. It is internally configured as 4 Banks of 2M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM63A165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

8.2 Features

Fast access time from clock: 5/5.4 ns

- Fast clock rate: 166/143 MHz
- Fully synchronous operation
- Internal pipelined architecture
- 4M word x 16-bit x 4-bank
- Programmable Mode registers
 - CAS Latency: 2, or 3
 - Burst Length: 1, 2, 4, 8, or full page
 - Burst Type: interleaved or linear burst
 - Burst stop function
- Auto Refresh and Self Refresh
- 8192 refresh cycles/64ms
- CKE power down mode
- Single +3.3V power supply
- Interface: LVTTTL
- 54-pin 400 mil plastic TSOP II package
 - Pb free and Halogen free

9. SAW FILTER

9.1 IF Filter for Audio Applications – Epcos K9656M

9.1.1 Standarts

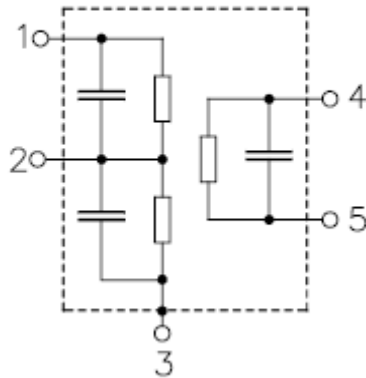
- B/G
- D/K
- I
- L/L'

9.1.2 Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L' - NICAM)
- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

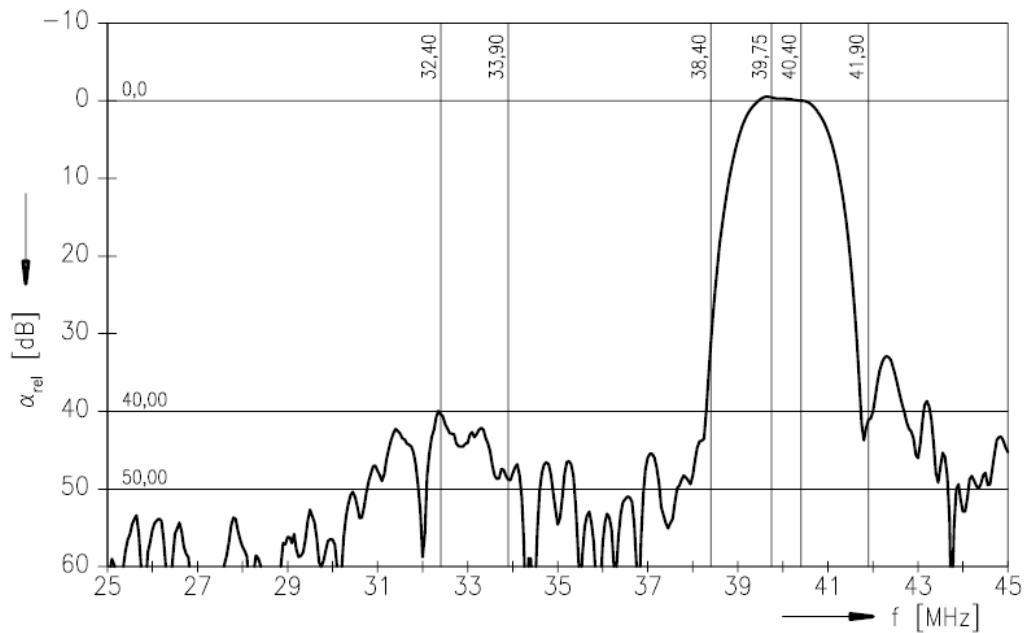
9.1.3 Pin Configuration

- 1 Input
- 2 Switching input
- 3 Chip carrier - ground
- 4 Output
- 5 Output

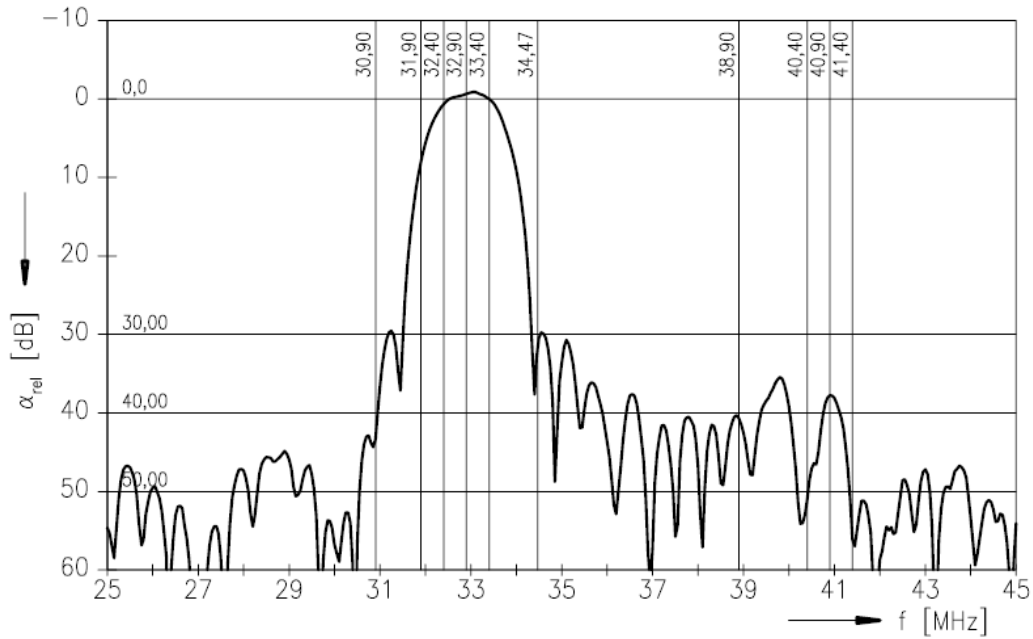


9.1.4 Frequency Response

Frequency Response of Channel 1:



Frequency Response of Channel 2:



9.2 IF Filter for Video Applications – Epcos K3958M

9.2.1 Standarts

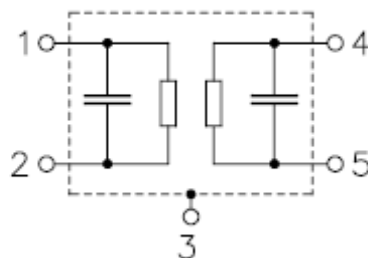
- B/G
- D/K
- I
- L/L'

9.2.2 Features

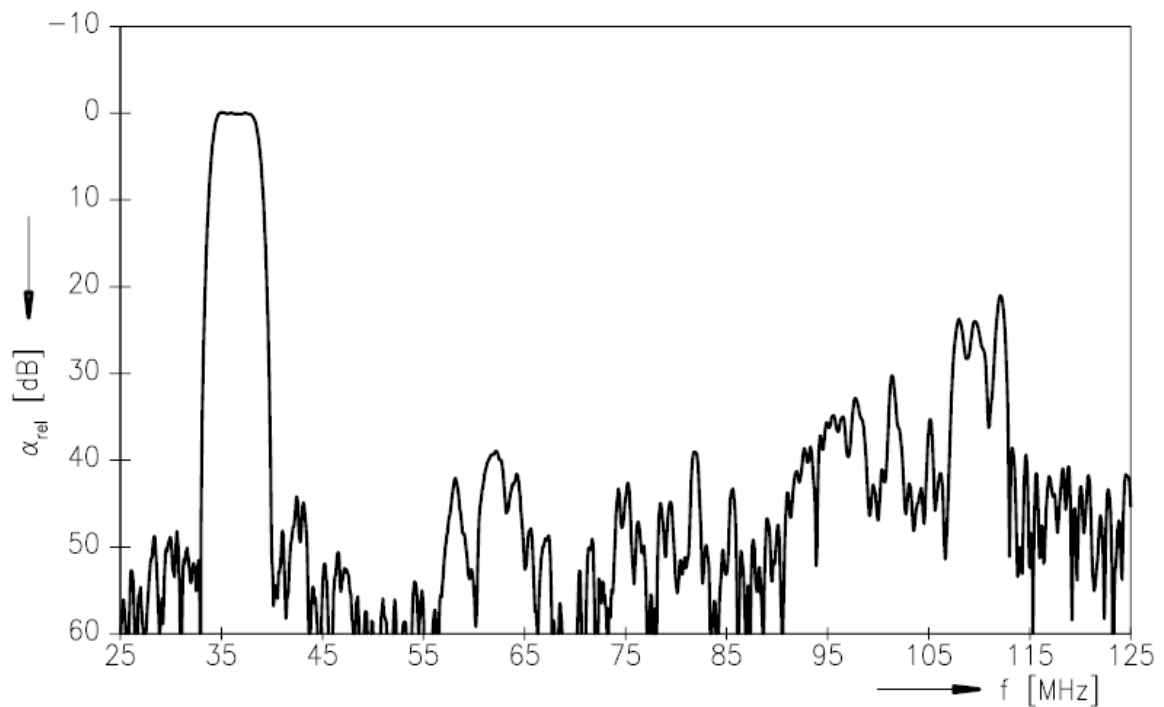
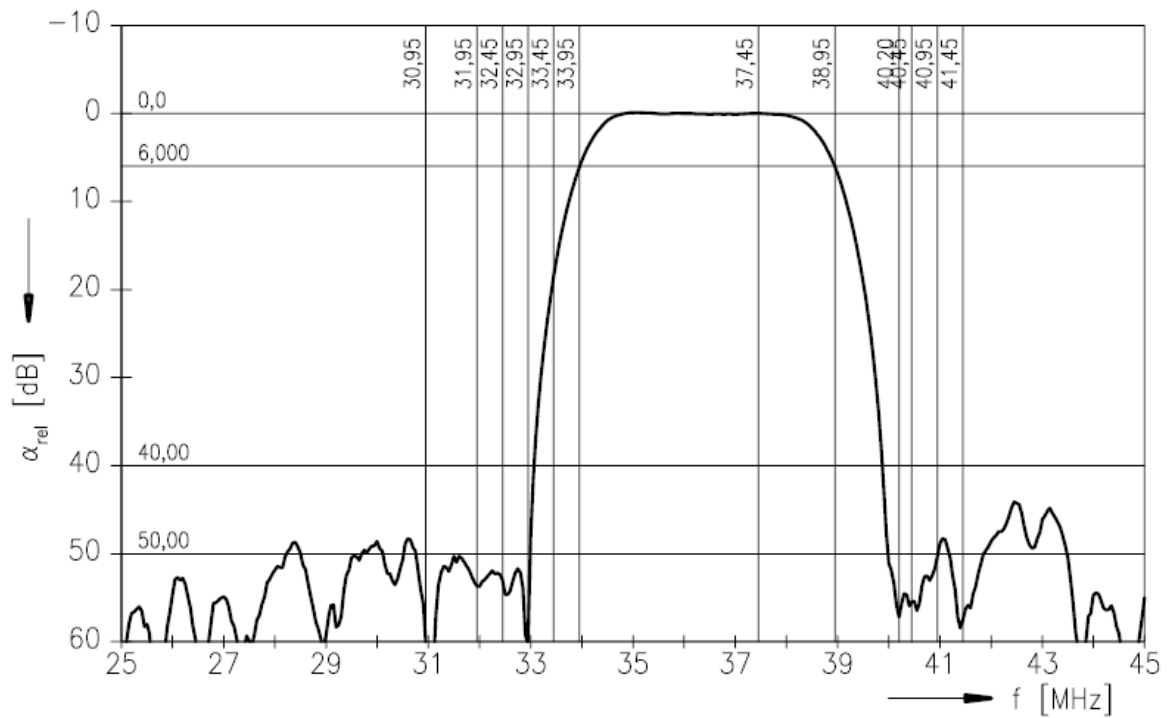
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

9.2.3 Pin Configuration

- 1 Input
- 2 Input - ground
- 3 Chip - carrier ground
- 4 Output
- 5 Output



9.2.4 Frequency Response



10. POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by an external power supply unit or produced on the chassis if an adapter is used for the supply. The 12V dc voltage is switched by IRF 7314 power mosfet in TV sets with mechanical switch to produce the required standby voltage. Also regulators and mosfets generate 1.8V, 3.3V and 5V and 1.26V voltages for other different parts of the chassis.

11. IC SPECIFICATIONS

11.1 32K Smart Serial EEPROM – 24C32

General Description

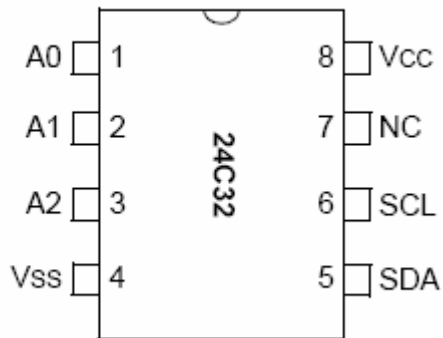
The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

Features

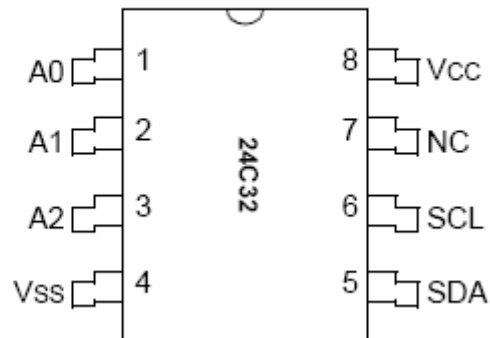
- Voltage operating range: 4.5V to 5.5V
- Peak write current 3 mA at 5.5V
- Maximum read current 150 μ A at 5.5V
- Standby current 1 μ A typical
- Industry standard two-wire bus protocol, I2C compatible
- Including 100 kHz and 400 kHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance: 10,000,000 Erase/Write cycles guaranteed for High Endurance Block, 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges: Commercial (C): 0°C to +70°C, Industrial (I): -40°C to +85°C

Pin Configuration

PDIP



SOIC



Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	No Internal Connection

11.2 TL062

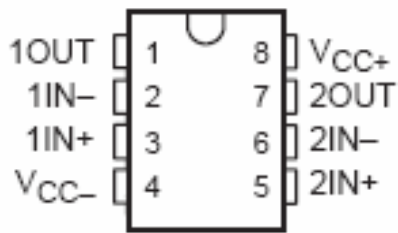
General Description

Low-power JFET-input operational amplifier

Features

- Very Low Power Consumption
- Typical Supply Current . . . 200 μ A (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes VCC+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/ μ s Typ

Pin Configuration



11.3 PI5V330

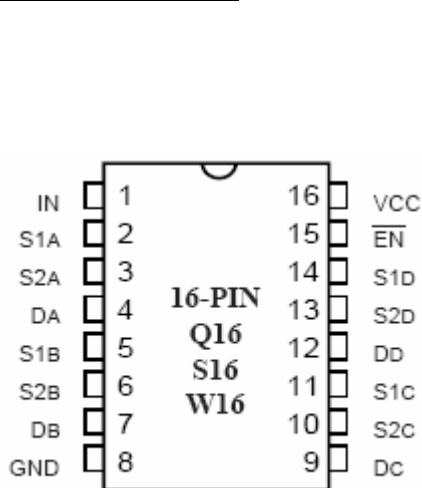
General Description

Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance. The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch can be driven from a current output RAMDAC or voltage output composite video source. Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation. The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

Features

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: .58 dB
- Ultra-low quiescent power (0.1 μ A typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
 - 16-pin 300-mil wide plastic SOIC (S)
 - 16-pin 150-mil wide plastic SOIC (W)
 - 16-pin 150-mil wide plastic QSOP (Q)

Pin Configuration



Pin Name	Description
S1A, S2A S1B, S2B S1C, S2C S1D, S2D	Analog Video I/O
IN	Select Input
$\overline{\text{EN}}$	Enable
DA, DB, DC, DD	Analog Video I/O
GND	Ground
VCC	Power

11.4 74HCT4053

General Description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A. The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input (E). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (Sn). With E LOW, one of the two switches is selected (low-impedance ON-state) by S1 to S3. With E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. VCC and GND are the supply voltage pins for the digital control inputs (S1 to S3 and E). The VCC to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC - VEE may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

Features

- Low ON resistance:
- 80 W (typical) at VCC - VEE = 4.5 V
- 70 W (typical) at VCC - VEE = 6.0 V
- 60 W (typical) at VCC - VEE = 9.0 V
- Logic level translation:
- To enable 5 V logic to communicate with ± 5 V analog signals
- Typical 'break before make' built in
- Complies with JEDEC standard no. 7A
- ESD protection: HBM EIA/JESD22-A114-C exceeds 2000 V, MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

Pin Configuration

Symbol	Pin	Description
2Y1	1	2 independent input/output 1
2Y0	2	2 independent input/output 0
3Y1	3	3 independent input/output 1
3Z	4	3 common input/output
3Y0	5	3 independent input/output 0
E	6	enable input (active LOW)
V _{EE}	7	negative supply voltage
GND	8	ground (0 V)
S3	9	select input 3
S2	10	select input 2
S1	11	select input 1
1Y0	12	1 independent input/output 0
1Y1	13	1 independent input/output 1
1Z	14	1 common input/output
2Z	15	2 common input/output
V _{CC}	16	supply voltage

11.5 FMS6145

General Description

The FMS6145 Low-Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Five 4th-order filters provide improved image quality compared to typical 2nd or 3rd-order passive solutions. The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required. The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

Features

- Five 4th-order 8MHz (SD) filters
- Drives single, AC- or DC-coupled, video loads (2V_{pp}, 150Ω)
- Drives dual, AC- or DC-coupled, video loads (2V_{pp}, 75Ω)
- Transparent input clamping
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Robust 8kV ESD protection
- Lead-free TSSOP-14 package

Pin Configuration

Pin #	Name	Type	Description
1	IN1	Input	Video input, channel 1
2	IN2	Input	Video input, channel 2
3	IN3	Input	Video input, channel 3
4	V _{CC}	Input	+5V supply, do not float
5	IN4	Input	Video input, channel 4
6	IN5	Input	Video input, channel 5
7, 8	NC		No Connect
9	OUT5	Output	Filtered video output, channel 5
10	OUT4	Output	Filtered video output, channel 4
11	GND	Output	Must be tied to ground, do not float
12	OUT3	Output	Filtered video output, channel 3
13	OUT2	Output	Filtered video output, channel 2
14	OUT1	Output	Filtered video output, channel 1

11.6 LM1117

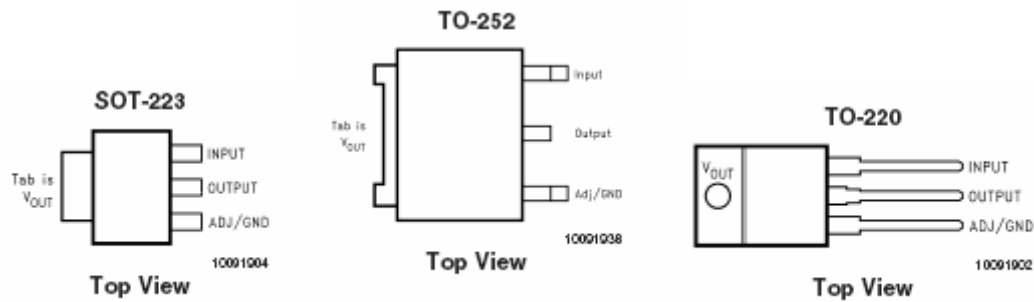
General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10 μ F tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

Pin Configuration



11.7 ST24LC21

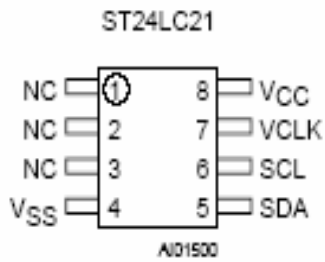
Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 Bits. This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Features

- 1 Million Erase/Write Cycles
- 40 Years Data Retention
- 2.5v To 5.5v Single Supply Voltage
- 400k Hz Compatibility Over The Full Range Of Supply Voltage
- Two Wire Serial Interface I2c Bus
- Compatible
- Page Write (Up To 8 Bytes)
- Byte, Random And Sequential Read
- Modes
- Self Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced Esd/Latch Up
- Performances

Pin Configuration



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I ² C mode)
V _{CC}	Supply Voltage
V _{SS}	Ground
VCLK	Clock Transmit only mode
WC	Write Control

11.8 24LC02

Description

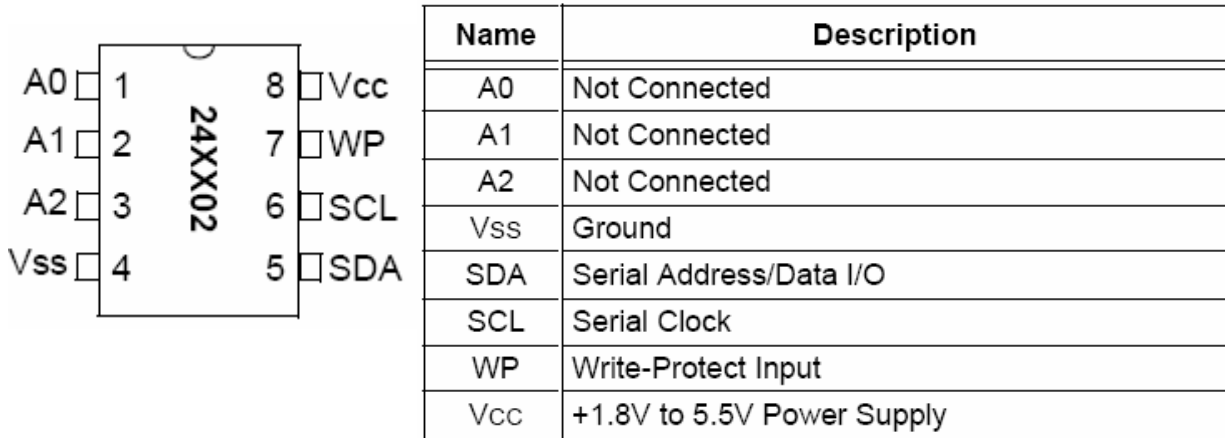
The Microchip Technology Inc. 24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 μ A and 1 mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data. The 24XX02 is available in the standard 8-pin PDIP, surface mount OIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

Features

- Single supply with operation down to 1.8V
- Low-power CMOS technology
 - 1 mA active current typical
 - 1 μ A standby current typical (I-temp)
- Organized as 1 block of 256 bytes (1 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 8 bytes
- 2 ms typical write cycle time for page write
- Hardware write-protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP packages
- 5-lead SOT-23 package
- Pb-free finish available
- Available for extended temperature ranges:

- Industrial (I): -40°C to +85°C
- Automotive (E): -40°C to +125°C

Pin Configuration



11.9 MAX810

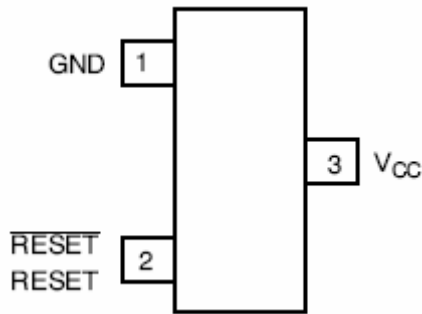
General Description

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required. The reset output is driven active within 10 μ sec of VCC falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low RESET output. Both devices are available in SOT-23 and SC-70 packages. The MAX809/810 are optimized to reject fast transient glitches on the VCC line. Low supply current of 0.5 μ A (VCC = 3.2 V) makes these devices suitable for battery powered applications.

Features

- Precision VCC Monitor for 1.5 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power-On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: -40°C to 105°C
- Pb-Free Packages are Available

Pin Configuration



11.10 TDA1308

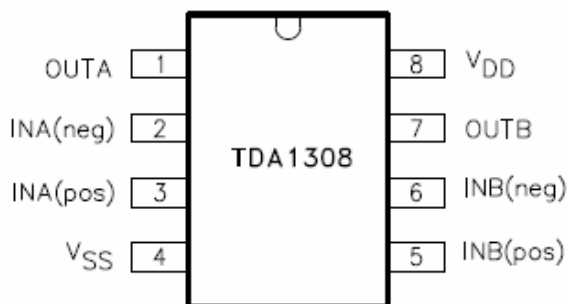
Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

Features

- Operating temperature range: -40 to +85 C
- No switch ON/OFF clicks
- Short-circuit resistant
- signal-to-noise ratio: 110 dB
- total harmonic distortion: 0.001 %

Pin Configuration



SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
VSS	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
VDD	8	positive supply

11.11 MP1583

General Description

The MP1583 is a step-down regulator with a built in internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal

shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20 μ A of supply current.

The MP1583 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

Features

- 3A Output Current
- Programmable Soft-Start
- 100m Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20 μ A Shutdown Mode
- Fixed 385KHz frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 23V operating Input Range
- Output Adjustable From 1.22 to 21V
- Under Voltage Lockout
- Available in 8 pin SOIC Package
- 3A Evaluation Board Available

Pin Configuration

#	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side n-channel MOSFET switch. Connect a 4.7nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See <i>Input Capacitor</i>
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. (Note: Connect the exposed pad on backside to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V. See <i>Setting the Output Voltage</i>
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See <i>Compensation</i>
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1 μ F capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

11.12 MP2112

General Description

The MP2112 is a 1MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for powering portable equipment that powered by a single cell Lithium-Ion (Li+) battery. The MP2112 can supply 1A of load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. The MP2112 can also run at 100% duty cycle for low dropout applications.

The MP2112 is available in a space-saving 6-pin QFN package.

Features

- High Efficiency: Up to 95%
- 1MHz Constant Switching Frequency
- 1A Available Load Current
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Control
- Short Circuit Protection
- Thermal Fault Protection
- <0.1 μ A Shutdown Current
- Space Saving 3mm x 3mm QFN6 Package

Pin Configuration

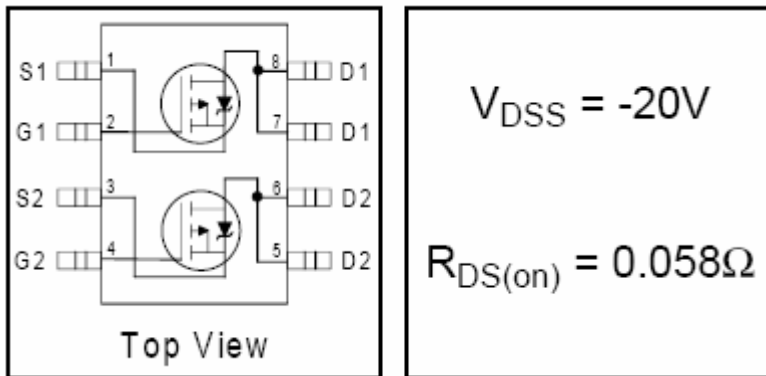
Pin #	Name	Description
1	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
2	GND	Ground.
3	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
4	VINB	Supply Input-Power.
5	VINA	Supply Input-Analog.
6	EN	Enable Input.

11.13 IRF7314

General Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.

Pin Configuration



12. SERVICE MENU SETTINGS

In order to reach service menu, First Press “MENU” Then press the remote control code, which is “4725”. In DTV mode, first press “MENU” and select “TV SETUP”. Then, press “4725”.

12.1. Video Setup

Panel Info <.....>

32_LC_SAC1

Blue Background <.....>

If “Menu” selected, “Blue Background” item is seen in “Feature” menu.

If “Yes” selected, “Blue Background” is on and not seen in “Feature” menu

Film Mode <.....>

If “Yes” selected, “Film Mode” feature is active.

Dynamic Contrast <.....>

If “Yes” selected, “Dynamic Contrast” feature is active.

Game Mode <.....>

If “Yes” selected, “Game Mode” feature is active

SRGB For PC <.....>

If “Yes” selected, PCs can use SRGB option.

Dynamic Noise Reduction<.....>

If “Yes” selected, “Dynamic Noise Reduction” feature is active

WSS Option<.....>

If “Yes” selected, WSS Option can be used

12.2. AudioSetup

BG<.....>

Europe

New Zealand
Australia
No

DK<.....>

I<.....>

L<.....>

Equalizer <.....>

If "Yes" selected, "**Equalizer**" item is seen in "**Sound**" menu.

Headphone <.....>

If "Yes" selected, "**Headphone**" item is seen in "**Sound**" menu.

Power On/Off Melody <.....>

If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.

Dynamic Bass <.....> Value between 0 to 12

Effect<.....> Value between 0 to 7

Audio Delay ,offset <.....> Value between 0 to 190

Audio Setup Cont...2

Carrier mute<.....> Value between 0 to 28

Headphone Sound Select <.....>

Always Active Select

Always Inactive Select

Menu

Always Main Menu

Always PIP/PAP Window

Sound Mode Detect Time <.....> Value between 0 to 255

Noise Reduction Threshold <.....> Value between 0 to 255

Noise Reduction Time <.....> Value between 0 to 15

AVL Attack Time <.....> Value between 0 to 255

AVL Release Time <.....> Value between 0 to 255

Prescales (AVL On)

FM Prescale<.....> Value between 0 to 255

AM Prescale <.....> Value between 0 to 255

NICAM Prescale <.....> Value between 0 to 255

SCART Prescale <.....> Value between 0 to 255

FAV Prescale <.....> Value between 0 to 255

DTV Prescale <.....> Value between 0 to 255

HDMI Prescale <.....> Value between 0 to 255

YPbPr/PC Prescale <.....> Value between 0 to 255

An. USB Prescale <.....> Value between 0 to 255

Dig. USB Prescale <.....> Value between 0 to 255

Prescales (AVL Off)

FM Prescale<.....> Value between 0 to 255

AM Prescale <.....> Value between 0 to 255

NICAM Prescale <.....> Value between 0 to 255

SCART Prescale <.....> Value between 0 to 255

FAV Prescale <.....> Value between 0 to 255

DTV Prescale <.....> Value between 0 to 255

HDMI Prescale <.....> Value between 0 to 255

YPbPr/PC Prescale <.....> Value between 0 to 255

An. USB Prescale <.....> Value between 0 to 255
Dig. USB Prescale <.....> Value between 0 to 255
Clipping Levels (AVL On)
FM Clipping <.....> Value between 0 to 255
AM Clipping <.....> Value between 0 to 255
NICAM Clipping <.....> Value between 0 to 255
SCART Clipping <.....> Value between 0 to 255
FAV Clipping <.....> Value between 0 to 255
DTV Clipping <.....> Value between 0 to 255
HDMI Clipping <.....> Value between 0 to 255
YPbPr/PC Clipping <.....> Value between 0 to 255
An. USB Clipping <.....> Value between 0 to 255
Dig. USB Clipping <.....> Value between 0 to 255
Clipping Levels (AVL Off)
FM Clipping <.....> Value between 0 to 255
AM Clipping <.....> Value between 0 to 255
NICAM Clipping <.....> Value between 0 to 255
SCART Clipping <.....> Value between 0 to 255
FAV Clipping <.....> Value between 0 to 255
DTV Clipping <.....> Value between 0 to 255
HDMI Clipping <.....> Value between 0 to 255
YPbPr/PC Clipping <.....> Value between 0 to 255
An. USB Clipping <.....> Value between 0 to 255
Dig. USB Clipping <.....> Value between 0 to 255

12.3. Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> Value between 0 to +200
Main Tuner Setup
Tuner Type
LC_TDTC_GXX1D
Thomson DTT7543X
Philips TD1318AF-3
Samsung DTOs403LH172A
Generic (Analog Only)
Control Byte <.....> Value between 0 to +255
BSW1 <.....> Value between 0 to +255
BSW2 <.....> Value between 0 to +255
BSW3 <.....> Value between 0 to +255
Low-Mid – Low Byte <.....>
Low-Mid – High Byte <.....>
Mid-High – Low Byte <.....>
Mid-High – High Byte <.....>
S Band TOP <.....>
VIF TOP <.....> Value between 0 to +15
VIF TOP SECAM <.....> Value between 0 to +15
VIF TOP DK<.....> Value between 0 to +15
Synch Threshold<.....> Value between 0 to +40

16.4. Options

Options-1

Power Up

Standby

Last state

TV Open Mode

Source

1st TV

Last Tv

First APS <.....>

If "Yes" selected, first time TV opens by asking APS.

APS Volume <.....> *Value between 0 to +63*

Burn In Mode <.....>

If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.

APS Test

Autostore <.....>

If "Yes" selected, Channel is automatically stored.

Unicode Enabled <.....>

If "Yes" selected, Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If "Yes" selected, Source List Menu appears on the screen when press "source" button.

RS232 for B2B <.....>

If "Yes" selected, Remote Control commands the TV via RS232 and vice versa.

RC Select <.....>

RC Group 1

RC Group 2

RC Group 3

RC Group 4

RC Group 5

RC Group 6

Double Digit Key <.....>

If "Yes" selected, Double Digit Button on RC activates.

Protection <.....>

If "Yes" selected, short circuit protection activates.

Led Type <.....>

1 Led 1 Color

1 Led 2 Color

2 Led 2 Color

1 Led 3 Color

2 Led 3 Color

200 Programme <.....>

If "Yes" selected, totally 200 programmes can be used.

TouchPad <.....>

If "Yes" selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> Value between 0 to +63

TXT Type <.....>

Fasttext&Toptext

No

Default

Fasttext

Toptext

TXT Language <.....>

Menu

West

East

Cyrillic

Turk/Gre

Arabic

Persian

Auto

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

Menu

16:9

4:3

Panaromic

14:9 Zoom

Menu Timeout <.....>

Menu

15 Sec

30 Sec

60 Sec

No Time

Backlight <.....>

If "Yes" selected, "**Backlight**" feature is active.

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

If "Yes" selected, "**Analog USB**" option is active.

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

If "Yes" selected, "**CEC**" feature is active.

Digital USB Hotplug <.....>

If "Yes" selected, "**Digital USB Hotplug**" feature is active.

PIP Options

Pip <.....>

AV PIP

No PIP

PC PIP

Hotel Options <.....>

Hotel TV <.....>

If "Yes" selected, "Hotel TV" feature is active.

IR Smartloader <.....>

If "Yes" selected, "IR Smartloader" feature is active.

16.5. External Source Settings

TV <.....>

DTV <.....>

Ext 2 <.....>

Ext 2 S <.....>

FAV <.....>

BAV <.....>

S-Video <.....>

HDMI 1 <.....>

HDMI 2 <.....>

HDMI 3 <.....>

HDMI 4 <.....>

YPbPr <.....>

PC <.....>

16.6. Preset

User Adj.

ADC Adj.

Service Adj.

All Adj.

Init Factory Channels.

16.7. NVM Edit

NVM-edit addr. (hex)

NVM-edit data (hex)

NVM-data dec

16.8. Programming

HDMI DDC Update Mode <.....>

HDCP Key Update Mode <.....>

Software Bypass <.....>

If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> *Value between 0 to +255*

Memory Clock Step <.....> *Value between 0 to +255*

DTV Download <.....>

If "On" selected, DTV software can be updated from SCART.

DSUB9 Download <.....>

If "On" selected, DTV software can be updated from DSUB9.

16.9. Diagnostic

Eeprom I2C

Tuner I2C

IF I2C

HDMI I2C

DTV RS232

16.10. Product Info

13. SOFTWARE UPDATE DESCRIPTION

13.1 17MB25 Analog Part Software Update With Bootloader Procedure

1.1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin" extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Allthough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.

2. The starting to download something : When chassis is powered up the menu key has to be pushed. Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart, dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8

Programming		
1. HDMI DDC Update Mode		Off
2. HDCP Key Update Mode		Off
3. Software Bypass		On
4. LVDS Clock Step		255
5. Memory Clock Step		255
6. DTV Download		Off

Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal. To download hdcp key press k or to download eeprom content press w.

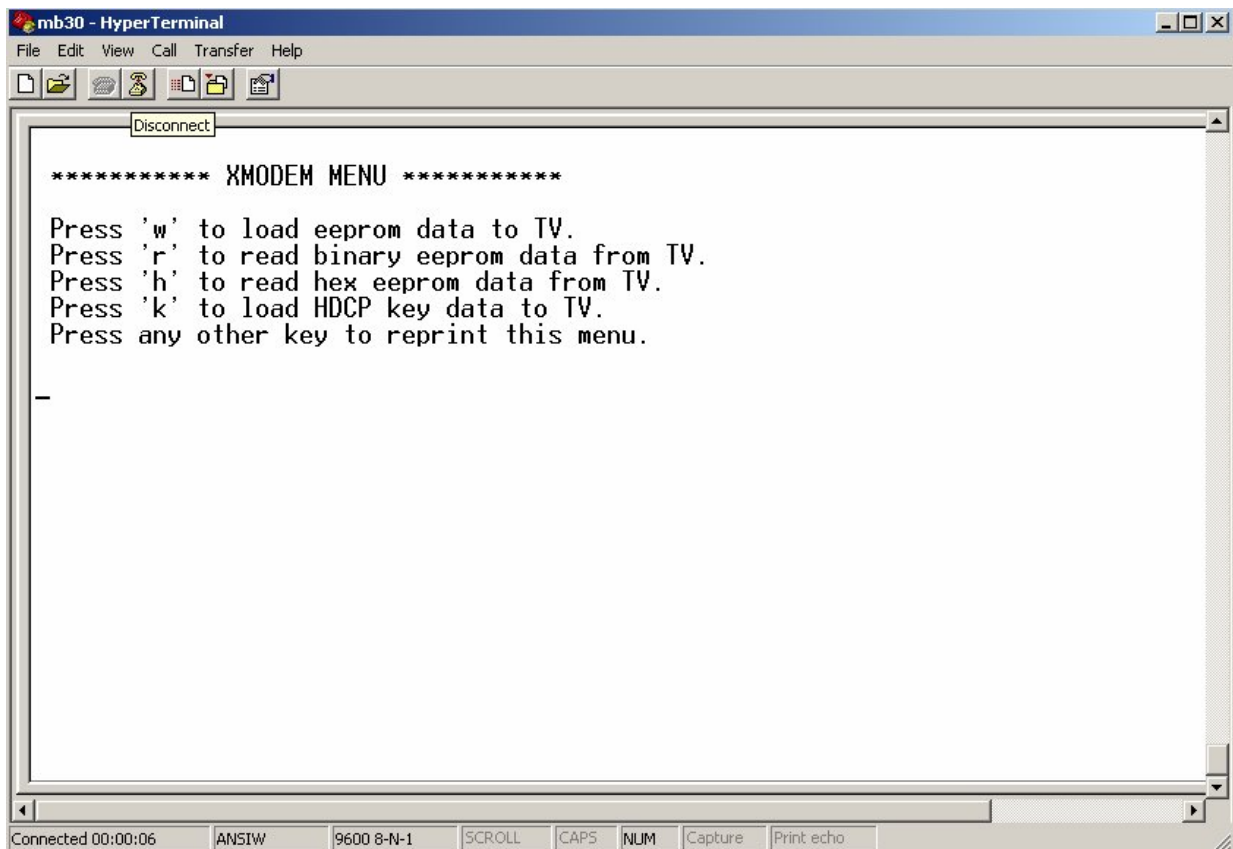


Figure 3. Xmodem Menu

If the repeated "C" characters are seen you can transfer file content via select Transfer->Send File and choose "Xmodem" protocol and click the "Send" button.

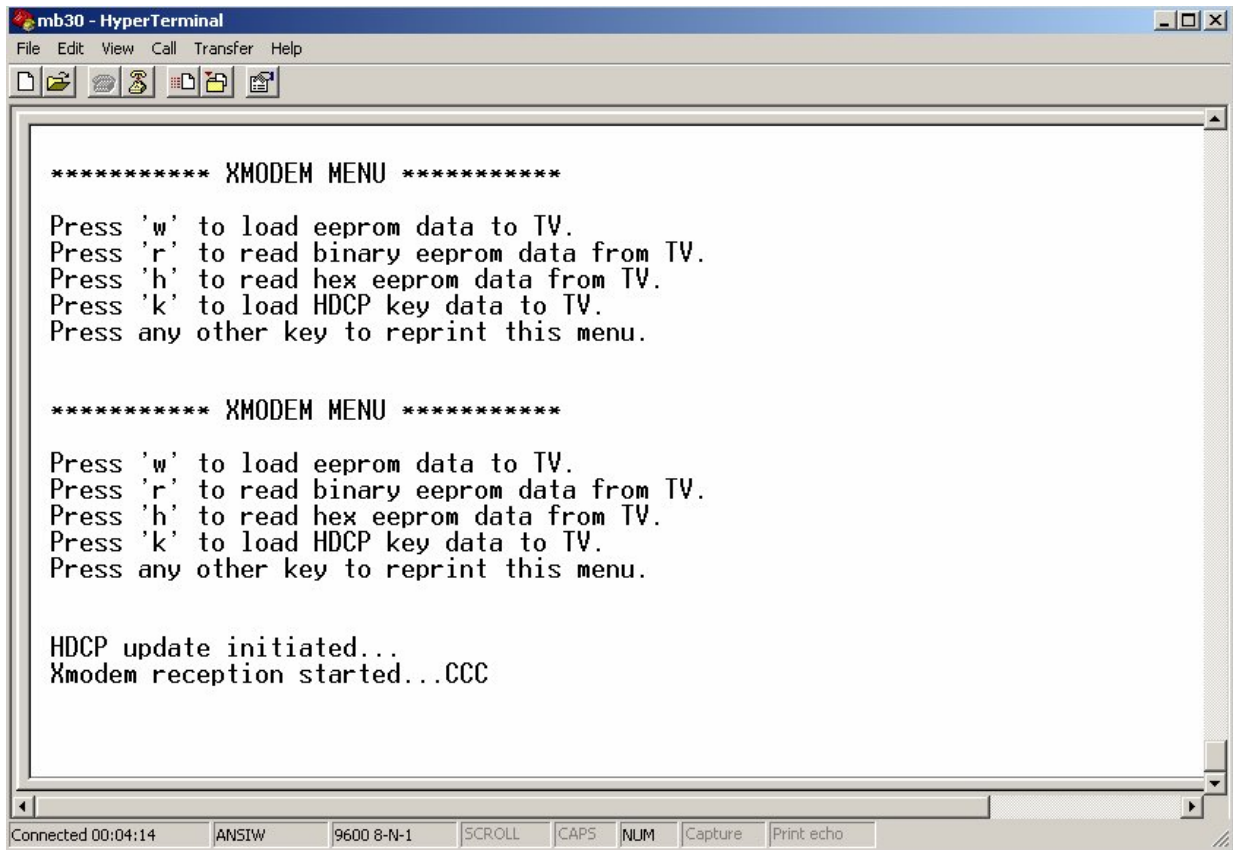


Figure 4. The Starting To Send

16.2 17MB25 HDCP key upload procedure.

- 1) Turn on TV set.
- 2) Open a COM connection using following parameters and select ISP COM Port No
Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None
- 3) Enter service menu by pressing "4" "7" "2" "5" consecutively while main menu is open
- 4) Select "9. Programming"
- 5) Select "HDMI HDCP Update Mode" yes.
- 6) On Hyper Terminal Window press "k"
- 7) Click on send file under Transfer Tab.
- 8) Select Xmodem and choose the HDCP key to be uploaded.
- 9) Press send button
- 10) Restart TV set

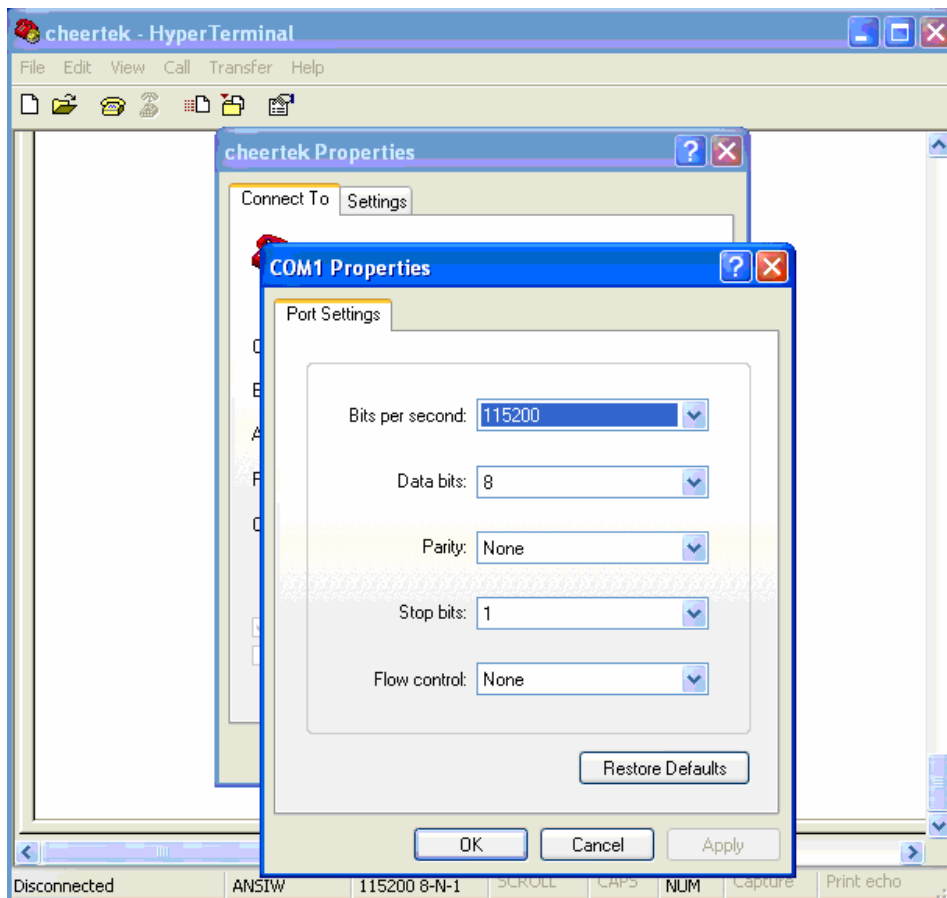
13.3 17MB25 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the "Tv Menu".
4. Enter "4725" for jumping to "Service Settings".
5. Select "8. Programming" step.
6. Change "6. DTV Download" to "On".
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the "MB25 SCART Interface" to SCART1 (bottom SCART plug).
2. Also connect the "MB25 SCART Interface" to PC.
3. Open "HyperTerminal".
4. Determine the "COM" settings listed and showed below.
 - Bit per second: 115200
 - Data bits: 8
 - Parity: None
 - Stop bits: 1
 - Flow control: None

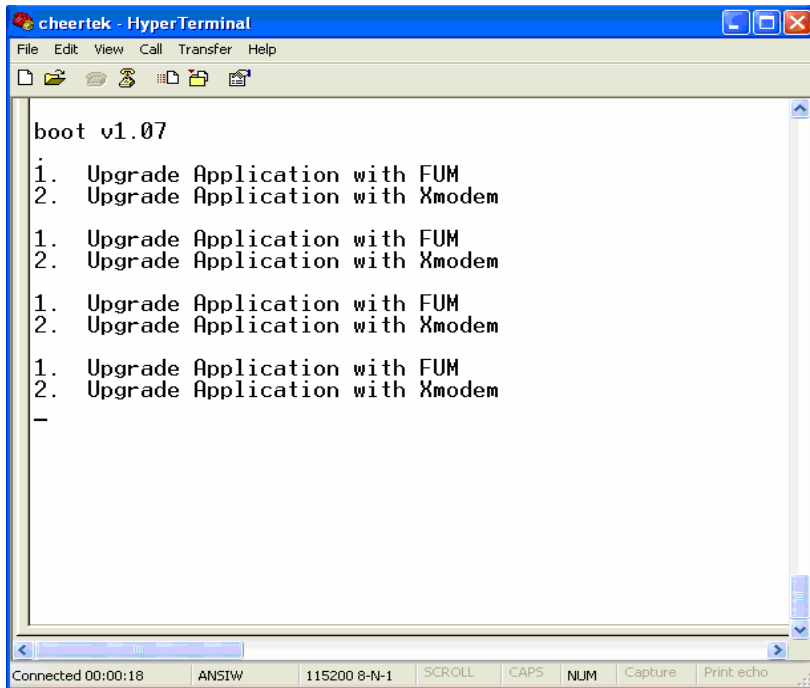


COM Properties Window

6. Click "OK".

Software Updating Procedure

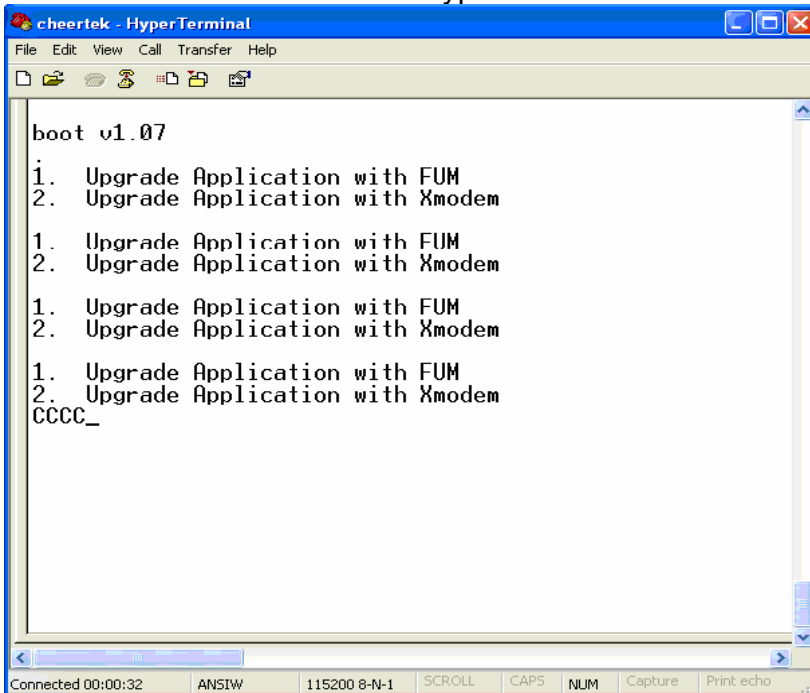
1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



```
cheertek - HyperTerminal
File Edit View Call Transfer Help
boot v1.07
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
-
```

Selection Window

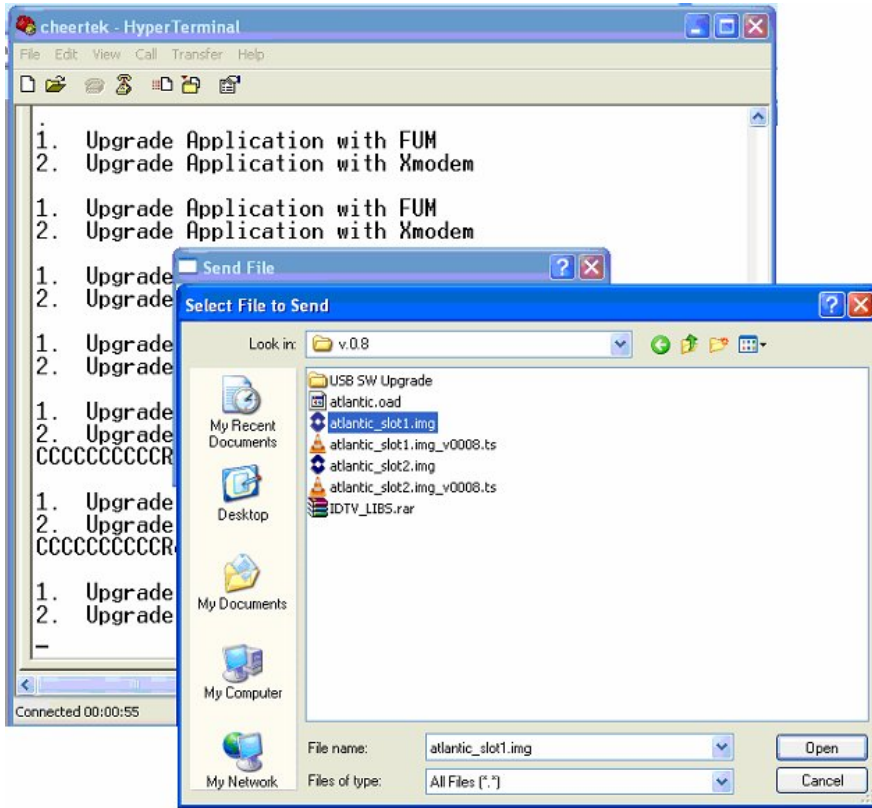
4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.



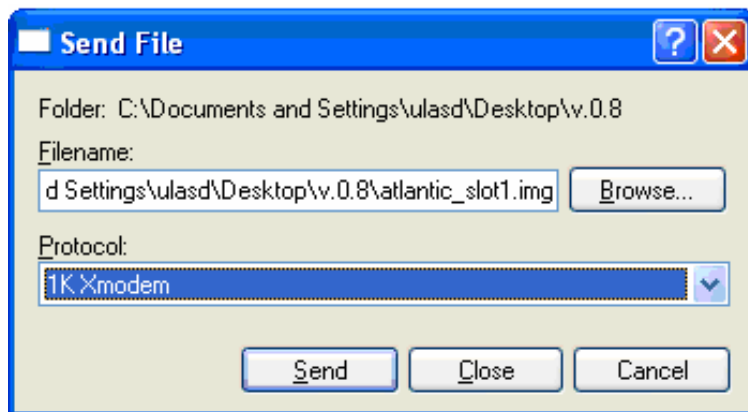
```
cheertek - HyperTerminal
File Edit View Call Transfer Help
boot v1.07
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
CCCC_
```

The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx_slot1.img**” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

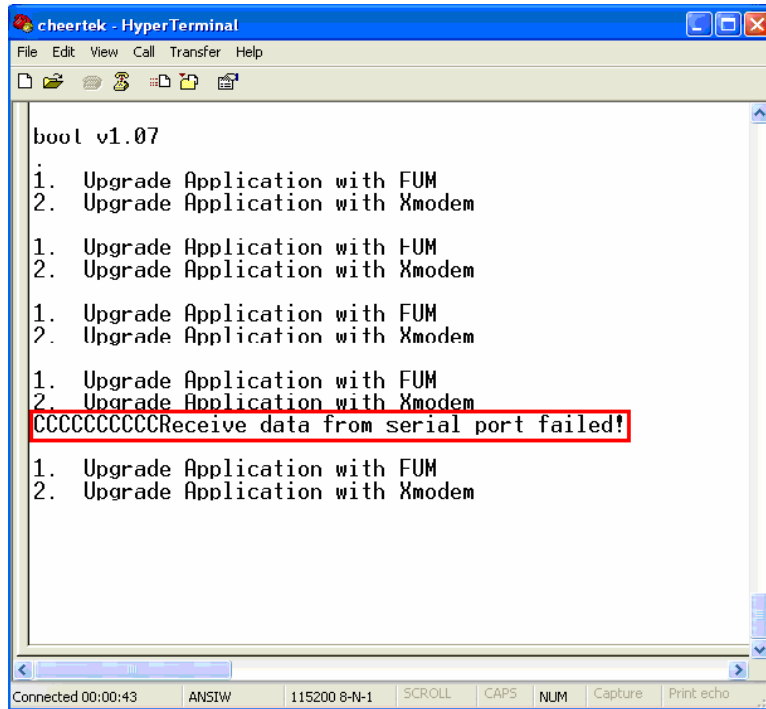


Selection of File



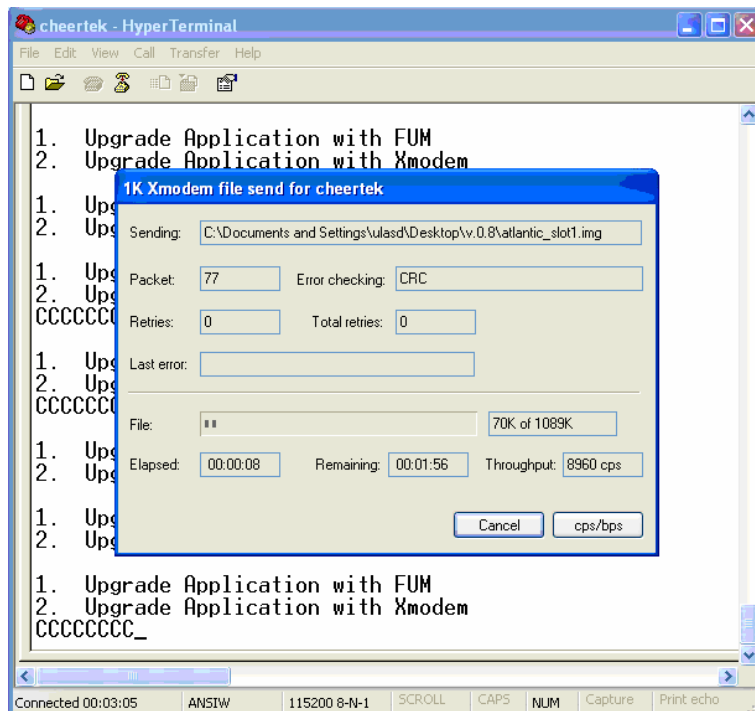
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



Capture of Receiving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

```
cheertek - HyperTerminal
File Edit View Call Transfer Help

erase sector 0x00050000...success
erase sector 0x00060000...success
erase sector 0x00070000...success
erase sector 0x00080000...success
erase sector 0x00090000...success
erase sector 0x000a0000...success
erase sector 0x000b0000...success
erase sector 0x000c0000...success
erase sector 0x000d0000...success
erase sector 0x000e0000...success
erase sector 0x000f0000...success
erase sector 0x00100000...success
erase sector 0x00110000...success
erase sector 0x00120000...success

Start to write to flash...

Write to flash finished

Please reboot the system!!

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem

Connected 00:05:44  ANSIV  115200 8-N-1  SCROLL  CAPS  NUM  Capture  Print echo
```

Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step X. Select the "Filename xxxx_slot2.img" using "Browse".
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.

```
cheertek - HyperTerminal
File Edit View Call Transfer Help

erase sector 0x00250000...success
erase sector 0x00260000...success
erase sector 0x00270000...success
erase sector 0x00280000...success
erase sector 0x00290000...success
erase sector 0x002a0000...success
erase sector 0x002b0000...success
erase sector 0x002c0000...success
erase sector 0x002d0000...success
erase sector 0x002e0000...success
erase sector 0x002f0000...success
erase sector 0x00300000...success
erase sector 0x00310000...success
erase sector 0x00320000...success

Start to write to flash...

Write to flash finished

Please reboot the system!!

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem

Connected 00:09:28  ANSIV  115200 8-N-1  SCROLL  CAPS  NUM  Capture  Print echo
```

End of The Sending Process

Checking Of The New Software

1. Turn off and on the TV.
2. Enter the "Setup" submenu in the "DTV Menu".
3. Choose the "Configuration" option.
4. For controlling new software, check the "Receiver Upgrade" option.

13.4 17MB25 Digital Software Update From USB

Software upgrade is possible via USB disk by following the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

Revert operation:

With revert operation, it is possible to *downgrade* the software.

Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

For controlling new software, check the "Receiver Upgrade" option.

New Zealand
Australia
No

DK<.....>

I<.....>

L<.....>

Equalizer <.....>

If "Yes" selected, "**Equalizer**" item is seen in "**Sound**" menu.

Headphone <.....>

If "Yes" selected, "**Headphone**" item is seen in "**Sound**" menu.

Power On/Off Melody <.....>

If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.

Dynamic Bass <.....> Value between 0 to 12

Effect<.....> Value between 0 to 7

Audio Delay ,offset <.....> Value between 0 to 190

Audio Setup Cont...2

Carrier mute<.....> Value between 0 to 28

Headphone Sound Select <.....>

Always Active Select

Always Inactive Select

Menu

Always Main Menu

Always PIP/PAP Window

Sound Mode Detect Time <.....> Value between 0 to 255

Noise Reduction Threshold <.....> Value between 0 to 255

Noise Reduction Time <.....> Value between 0 to 15

AVL Attack Time <.....> Value between 0 to 255

AVL Release Time <.....> Value between 0 to 255

Prescales (AVL On)

FM Prescale<.....> Value between 0 to 255

AM Prescale <.....> Value between 0 to 255

NICAM Prescale <.....> Value between 0 to 255

SCART Prescale <.....> Value between 0 to 255

FAV Prescale <.....> Value between 0 to 255

DTV Prescale <.....> Value between 0 to 255

HDMI Prescale <.....> Value between 0 to 255

YPbPr/PC Prescale <.....> Value between 0 to 255

An. USB Prescale <.....> Value between 0 to 255

Dig. USB Prescale <.....> Value between 0 to 255

Prescales (AVL Off)

FM Prescale<.....> Value between 0 to 255

AM Prescale <.....> Value between 0 to 255

NICAM Prescale <.....> Value between 0 to 255

SCART Prescale <.....> Value between 0 to 255

FAV Prescale <.....> Value between 0 to 255

DTV Prescale <.....> Value between 0 to 255

HDMI Prescale <.....> Value between 0 to 255

YPbPr/PC Prescale <.....> Value between 0 to 255

An. USB Prescale <.....> Value between 0 to 255
Dig. USB Prescale <.....> Value between 0 to 255
Clipping Levels (AVL On)
FM Clipping <.....> Value between 0 to 255
AM Clipping <.....> Value between 0 to 255
NICAM Clipping <.....> Value between 0 to 255
SCART Clipping <.....> Value between 0 to 255
FAV Clipping <.....> Value between 0 to 255
DTV Clipping <.....> Value between 0 to 255
HDMI Clipping <.....> Value between 0 to 255
YPbPr/PC Clipping <.....> Value between 0 to 255
An. USB Clipping <.....> Value between 0 to 255
Dig. USB Clipping <.....> Value between 0 to 255
Clipping Levels (AVL Off)
FM Clipping <.....> Value between 0 to 255
AM Clipping <.....> Value between 0 to 255
NICAM Clipping <.....> Value between 0 to 255
SCART Clipping <.....> Value between 0 to 255
FAV Clipping <.....> Value between 0 to 255
DTV Clipping <.....> Value between 0 to 255
HDMI Clipping <.....> Value between 0 to 255
YPbPr/PC Clipping <.....> Value between 0 to 255
An. USB Clipping <.....> Value between 0 to 255
Dig. USB Clipping <.....> Value between 0 to 255

16.3. Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> Value between 0 to +200
Main Tuner Setup
Tuner Type
LC_TDTC_GXX1D
Thomson DTT7543X
Philips TD1318AF-3
Samsung DTOs403LH172A
Generic (Analog Only)
Control Byte <.....> Value between 0 to +255
BSW1 <.....> Value between 0 to +255
BSW2 <.....> Value between 0 to +255
BSW3 <.....> Value between 0 to +255
Low-Mid – Low Byte <.....>
Low-Mid – High Byte <.....>
Mid-High – Low Byte <.....>
Mid-High – High Byte <.....>
S Band TOP <.....>
VIF TOP <.....> Value between 0 to +15
VIF TOP SECAM <.....> Value between 0 to +15
VIF TOP DK <.....> Value between 0 to +15
Synch Threshold <.....> Value between 0 to +40

16.4. Options

Options-1

Power Up

Standby

Last state

TV Open Mode

Source

1st TV

Last Tv

First APS <.....>

If "Yes" selected, first time TV opens by asking APS.

APS Volume <.....> *Value between 0 to +63*

Burn In Mode <.....>

If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.

APS Test

Autostore <.....>

If "Yes" selected, Channel is automatically stored.

Unicode Enabled <.....>

If "Yes" selected,Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If "Yes" selected, Sorce List Menu appears on the screen when press "source" button.

RS232 for B2B <.....>

If "Yes" selected, Remote Control commandsthe TV via RS232 and vice versa.

RC Select <.....>

RC Group 1

RC Group 2

RC Group 3

RC Group 4

RC Group 5

RC Group 6

Double Digit Key <.....>

If "Yes" selected, Double Digit Button on RC activates.

Protection <.....>

If "Yes" selected,short circuit protection activates.

Led Type <.....>

1 Led 1 Color

1 Led 2 Color

2 Led 2 Color

1 Led 3 Color

2 Led 3 Color

200 Programme <.....>

If "Yes" selected, totaly 200 programmes can be used.

TouchPad <.....>

If "Yes" selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> Value between 0 to +63

TXT Type <.....>

Fasttext&Toptext

No

Default

Fasttext

Toptext

TXT Language <.....>

Menu

West

East

Cyrillic

Turk/Gre

Arabic

Persian

Auto

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

Menu

16:9

4:3

Panaromic

14:9 Zoom

Menu Timeout <.....>

Menu

15 Sec

30 Sec

60 Sec

No Time

Backlight <.....>

If "Yes" selected, "**Backlight**" feature is active.

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

If "Yes" selected, "**Analog USB**" option is active.

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

If "Yes" selected, "**CEC**" feature is active.

Digital USB Hotplug <.....>

If "Yes" selected, "**Digital USB Hotplug**" feature is active.

PIP Options

Pip <.....>

AV PIP

No PIP

PC PIP

Hotel Options <.....>

Hotel TV <.....>

If "Yes" selected, "Hotel TV" feature is active.

IR Smartloader <.....>

If "Yes" selected, "IR Smartloader" feature is active.

16.5. External Source Settings

TV <.....>

DTV <.....>

Ext 2 <.....>

Ext 2 S <.....>

FAV <.....>

BAV <.....>

S-Video <.....>

HDMI 1 <.....>

HDMI 2 <.....>

HDMI 3 <.....>

HDMI 4 <.....>

YPbPr <.....>

PC <.....>

16.6. Preset

User Adj.

ADC Adj.

Service Adj.

All Adj.

Init Factory Channels.

16.7. NVM Edit

NVM-edit addr. (hex)

NVM-edit data (hex)

NVM-data dec

16.8. Programming

HDMI DDC Update Mode <.....>

HDCP Key Update Mode <.....>

Software Bypass <.....>

If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> Value between 0 to +255

Memory Clock Step <.....> Value between 0 to +255

DTV Download <.....>

If "On" selected, DTV software can be updated from SCART.

DSUB9 Download <.....>

If "On" selected, DTV software can be updated from DSUB9.

16.9. Diagnostic

Eeprom I2C

Tuner I2C

IF I2C

HDMI I2C

DTV RS232

16.10. Product Info

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2. The Config Binary File : It has ".cin" extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Allthough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.

2. The starting to download something : When chassis is powered up the menu key has to be pushed. Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart, dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8

- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader software puts “C” character to uart. After repeating “C” characters are seen in the hyperterminal user can send any file to chassis by selecting Transfer -> Send File menu item and choosing “1K Xmodem” from protocol section.

```

<ïï0-³<<ïç0<-ï0<ïï
Clock change was finished
End of change frequency
DRAM writing....
DRAM reading...
DRAM BIST pass...2,36,EF,2,35,66,22,22,22,FF,FF,2,37,9F,FF,FF,
55,55,55,55,55,55,55,55,55,55,55,55,55,55,55,55,
APP_CheckDevice

ConnectStatus:0USB not connect
APP_CheckDevice

ConnectStatus:0USB not connect
APP_CheckDevice

ConnectStatus:0USB not connect
CCCC_

```

Figure 1. The Sample Output Before Sending The File

2. EEPROM update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used. Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is chosen in the service menu and switch “HDCP Key Update Mode” from off to on.

Programming		
1. HDMI DDC Update Mode		Off
2. HDCP Key Update Mode		Off
3. Software Bypass		On
4. LVDS Clock Step		255
5. Memory Clock Step		255
6. DTV Download		Off

Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal. To download hdcp key press k or to download eeprom content press w.

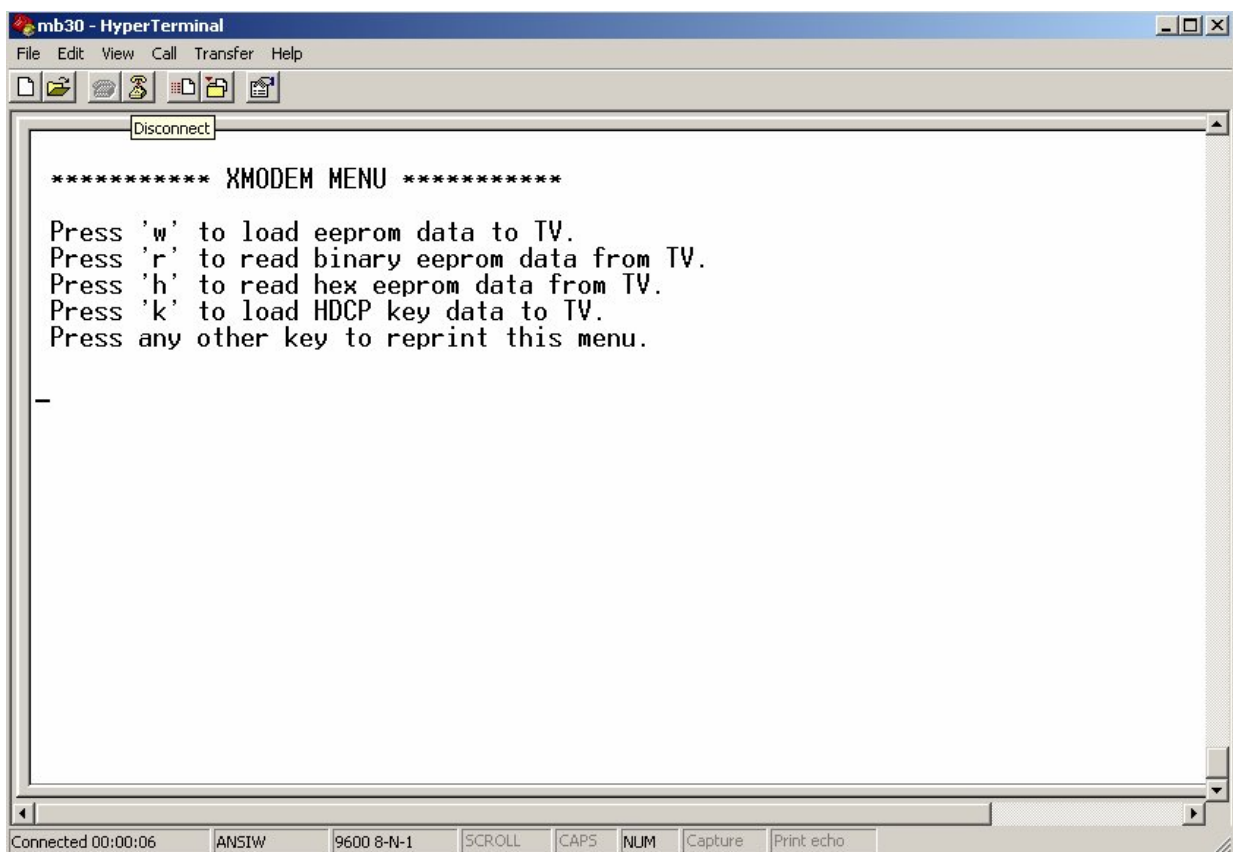


Figure 3. Xmodem Menu

If the repeated "C" characters are seen you can transfer file content via select Transfer->Send File and choose "Xmodem" protocol and click the "Send" button.

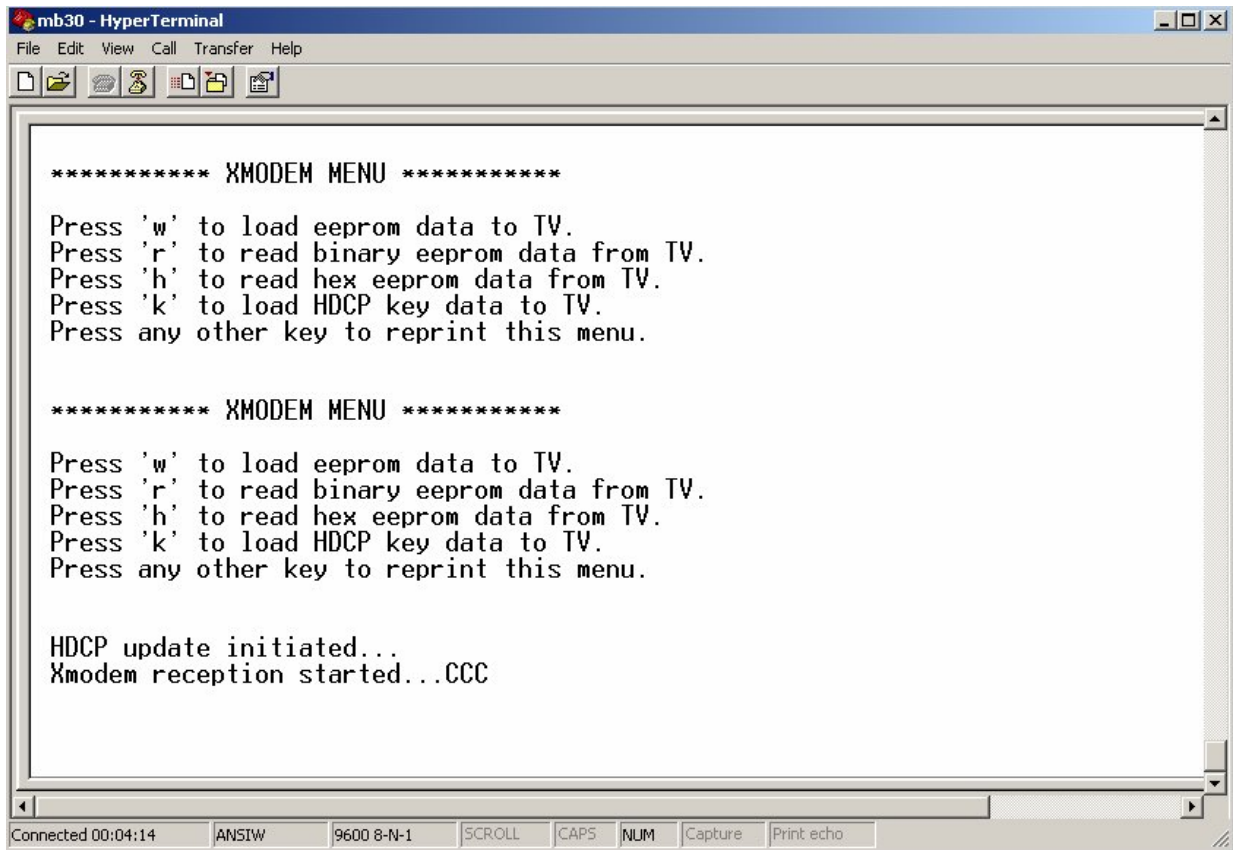


Figure 4. The Starting To Send

16.2 17MB25 HDCP key upload procedure.

- 1) Turn on TV set.
- 2) Open a COM connection using following parameters and select ISP COM Port No
Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None
- 3) Enter service menu by pressing "4" "7" "2" "5" consecutively while main menu is open
- 4) Select "9. Programming"
- 5) Select "HDMI HDCP Update Mode" yes.
- 6) On Hyper Terminal Window press "k"
- 7) Click on send file under Transfer Tab.
- 8) Select Xmodem and choose the HDCP key to be uploaded.
- 9) Press send button
- 10) Restart TV set

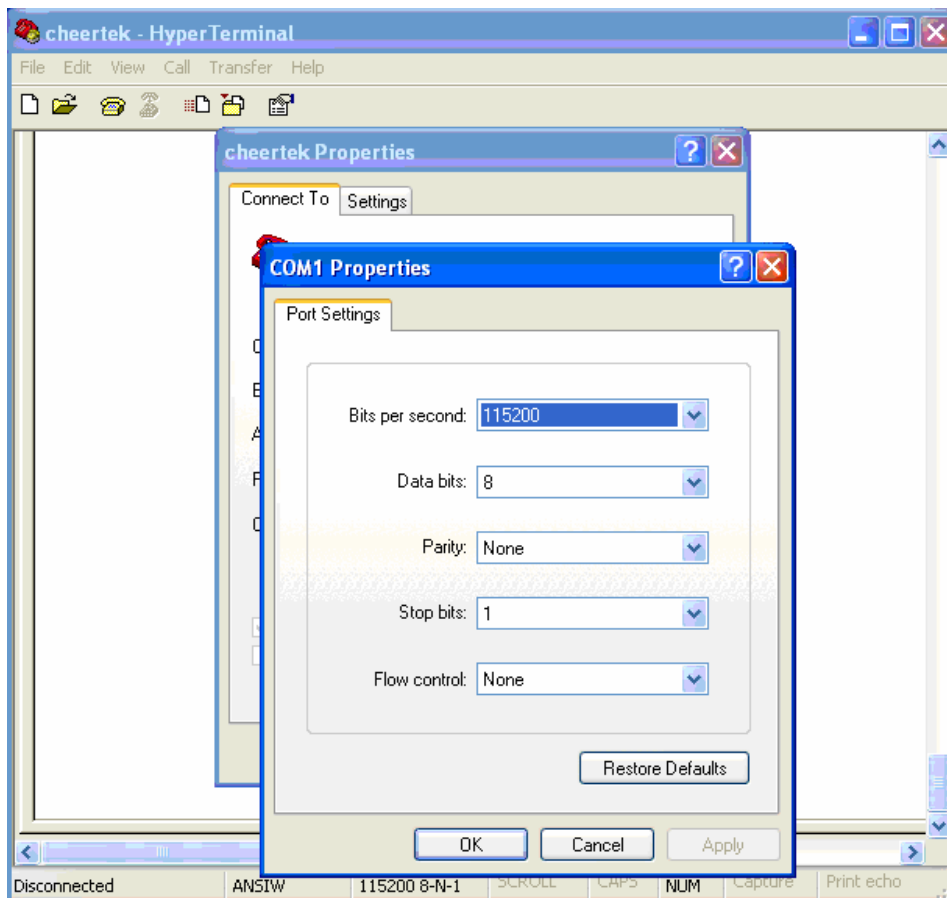
16.3 17MB25 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the "Tv Menu".
4. Enter "4725" for jumping to "Service Settings".
5. Select "8. Programming" step.
6. Change "6. DTV Download" to "On".
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the "MB25 SCART Interface" to SCART1 (bottom SCART plug).
2. Also connect the "MB25 SCART Interface" to PC.
3. Open "HyperTerminal".
4. Determine the "COM" settings listed and showed below.
 - Bit per second: 115200
 - Data bits: 8
 - Parity: None
 - Stop bits: 1
 - Flow control: None

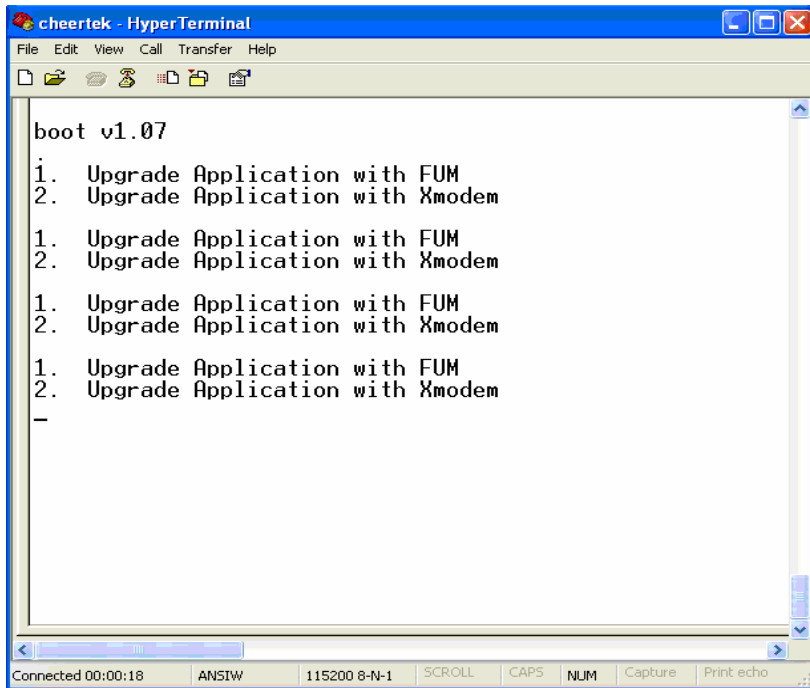


COM Properties Window

6. Click "OK".

Software Updating Procedure

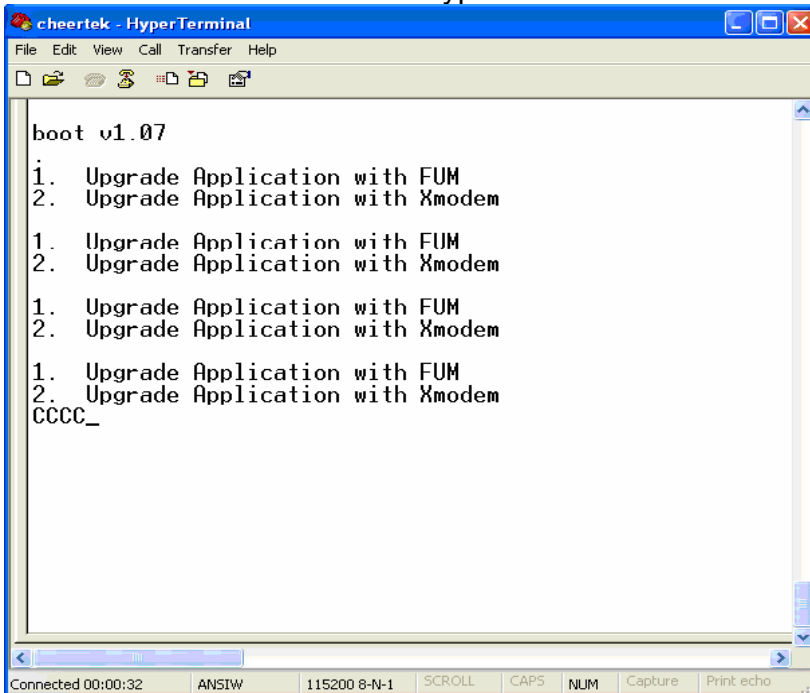
1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



```
cheertek - HyperTerminal
File Edit View Call Transfer Help
boot v1.07
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
-
```

Selection Window

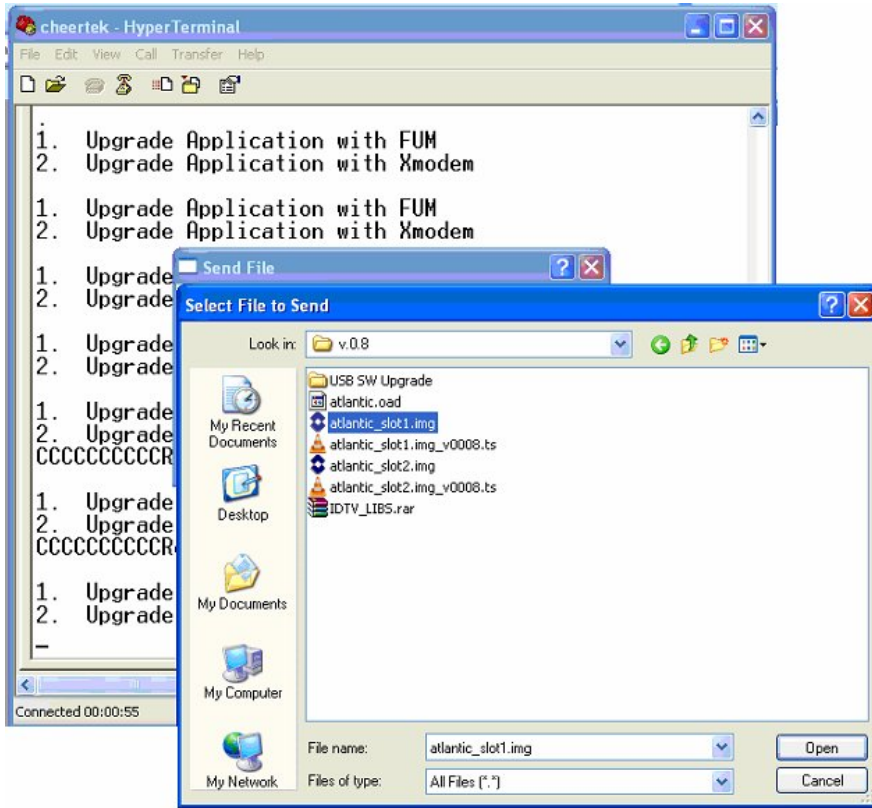
4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.



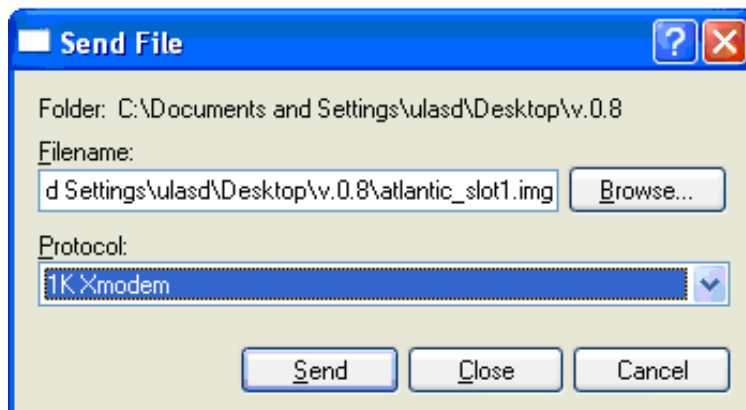
```
cheertek - HyperTerminal
File Edit View Call Transfer Help
boot v1.07
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem
CCCC_
```

The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx_slot1.img**” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

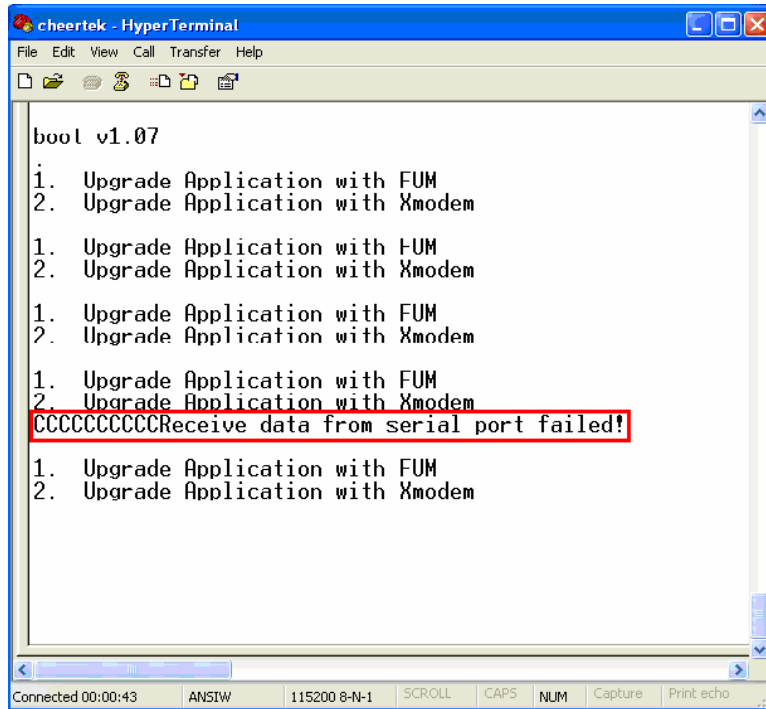


Selection of File



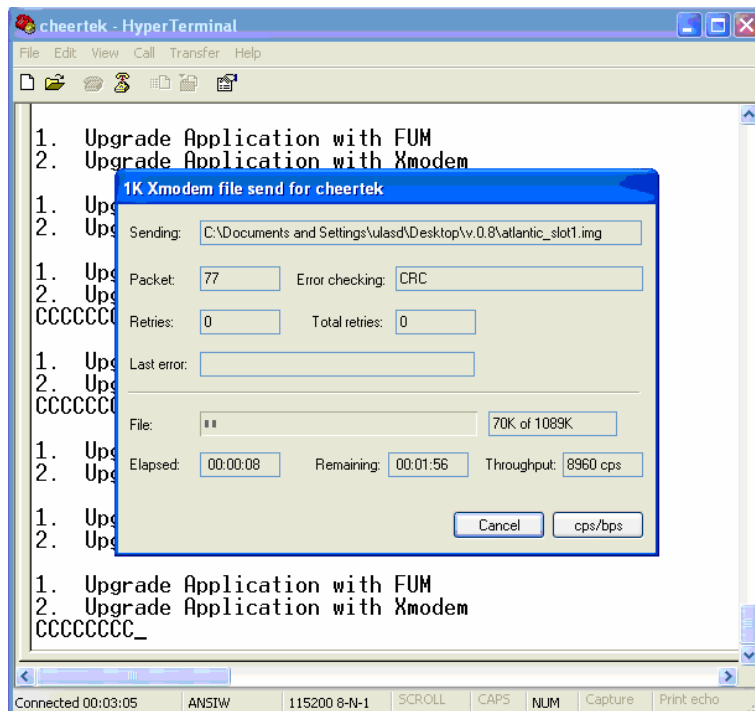
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



Capture of Receiving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

```
cheertek - HyperTerminal
File Edit View Call Transfer Help

erase sector 0x00050000...success
erase sector 0x00060000...success
erase sector 0x00070000...success
erase sector 0x00080000...success
erase sector 0x00090000...success
erase sector 0x000a0000...success
erase sector 0x000b0000...success
erase sector 0x000c0000...success
erase sector 0x000d0000...success
erase sector 0x000e0000...success
erase sector 0x000f0000...success
erase sector 0x00100000...success
erase sector 0x00110000...success
erase sector 0x00120000...success

Start to write to flash...

Write to flash finished

Please reboot the system!!

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem

Connected 00:05:44  ANSIV  115200 8-N-1  SCROLL  CAPS  NUM  Capture  Print echo
```

Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step X. Select the "Filename xxxx_slot2.img" using "Browse".
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.

```
cheertek - HyperTerminal
File Edit View Call Transfer Help

erase sector 0x00250000...success
erase sector 0x00260000...success
erase sector 0x00270000...success
erase sector 0x00280000...success
erase sector 0x00290000...success
erase sector 0x002a0000...success
erase sector 0x002b0000...success
erase sector 0x002c0000...success
erase sector 0x002d0000...success
erase sector 0x002e0000...success
erase sector 0x002f0000...success
erase sector 0x00300000...success
erase sector 0x00310000...success
erase sector 0x00320000...success

Start to write to flash...

Write to flash finished

Please reboot the system!!

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem

Connected 00:09:28  ANSIV  115200 8-N-1  SCROLL  CAPS  NUM  Capture  Print echo
```

End of The Sending Process

Checking Of The New Software

1. Turn off and on the TV.
2. Enter the "Setup" submenu in the "DTV Menu".
3. Choose the "Configuration" option.
4. For controlling new software, check the "Receiver Upgrade" option.

16.4 17MB25 Digital Software Update From USB

Software upgrade is possible via USB disk by following the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

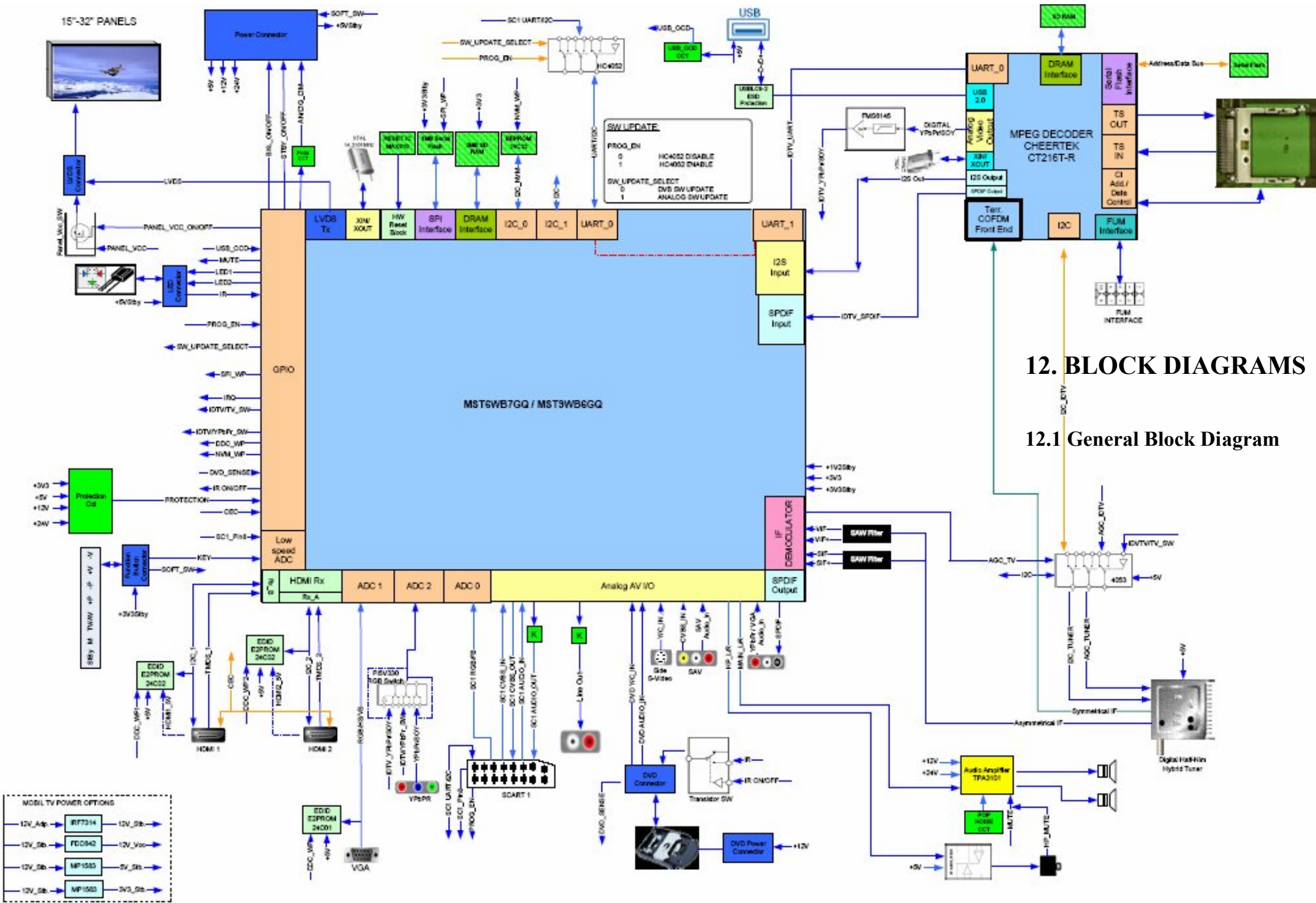
Revert operation:

With revert operation, it is possible to *downgrade* the software.

Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

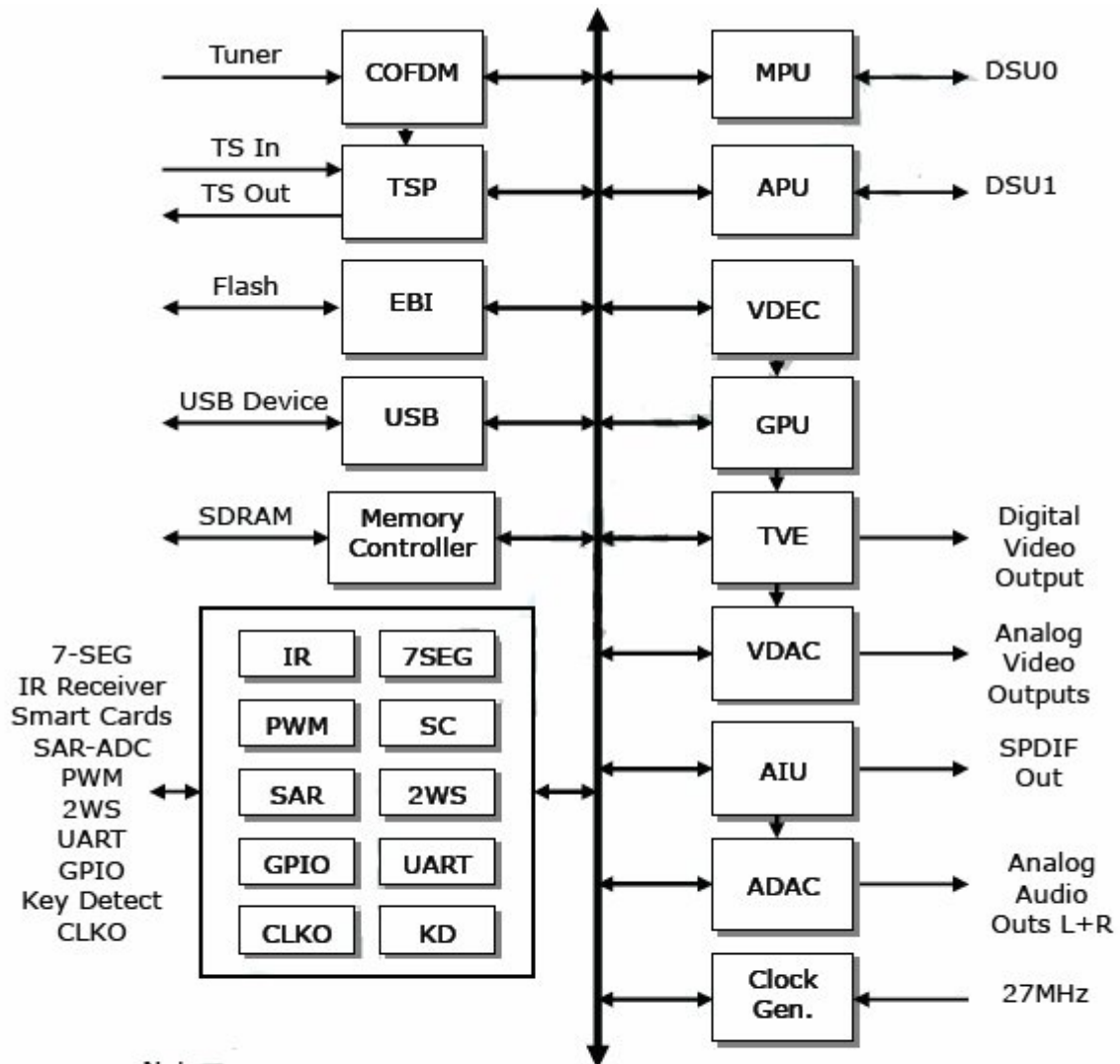
For controlling new software, check the "Receiver Upgrade" option.



12. BLOCK DIAGRAMS

12.1 General Block Diagram

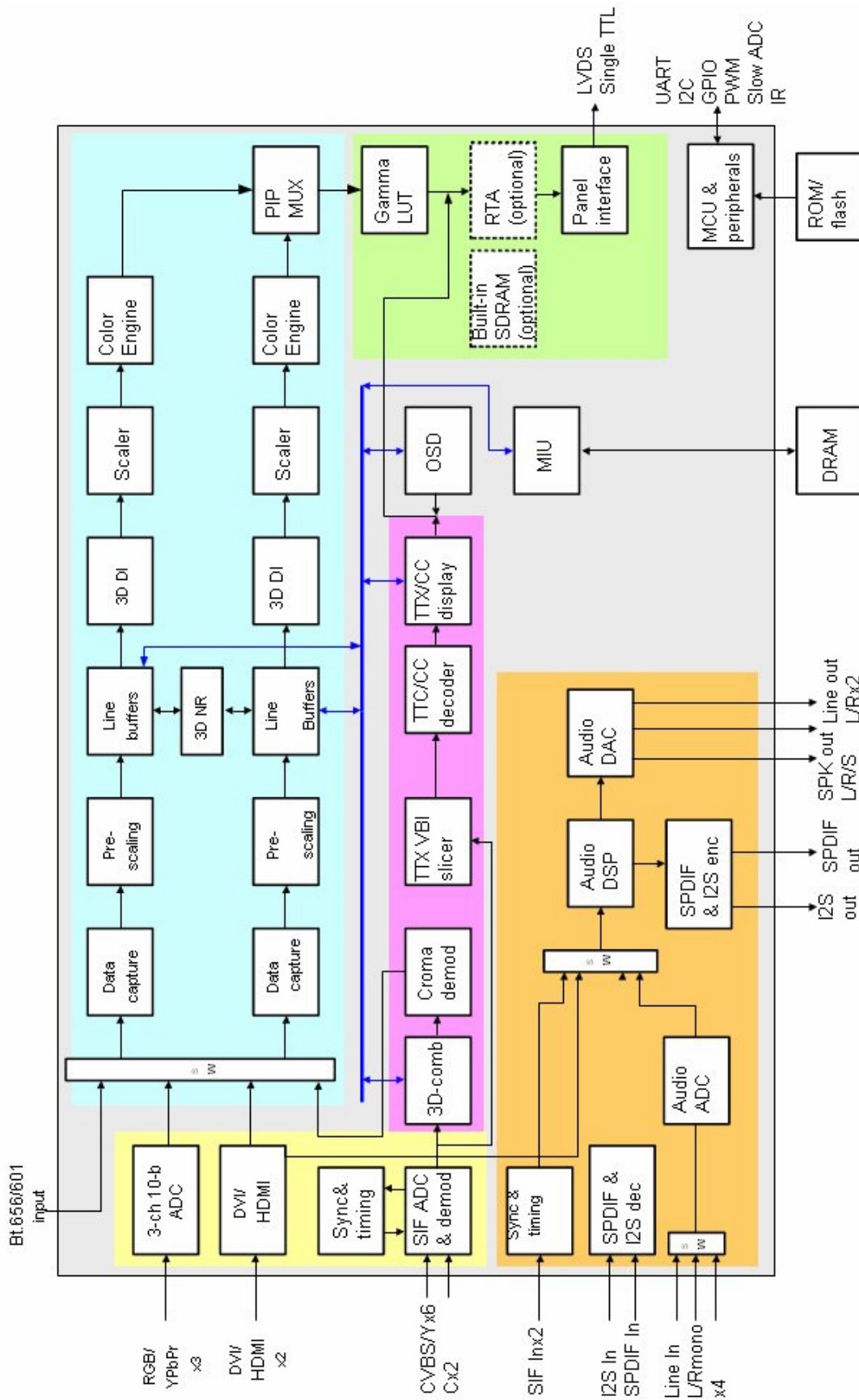
12.2 Integrated DVB-T Receiver Block Diagram

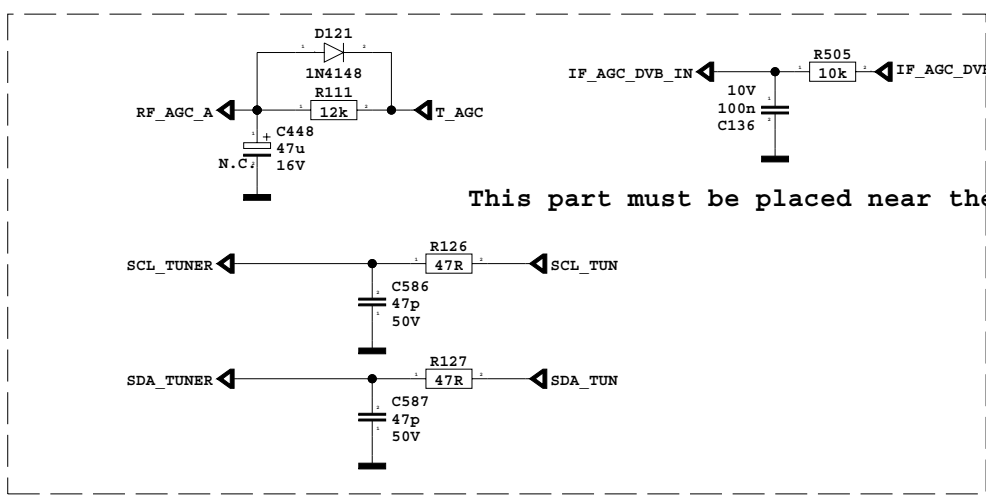
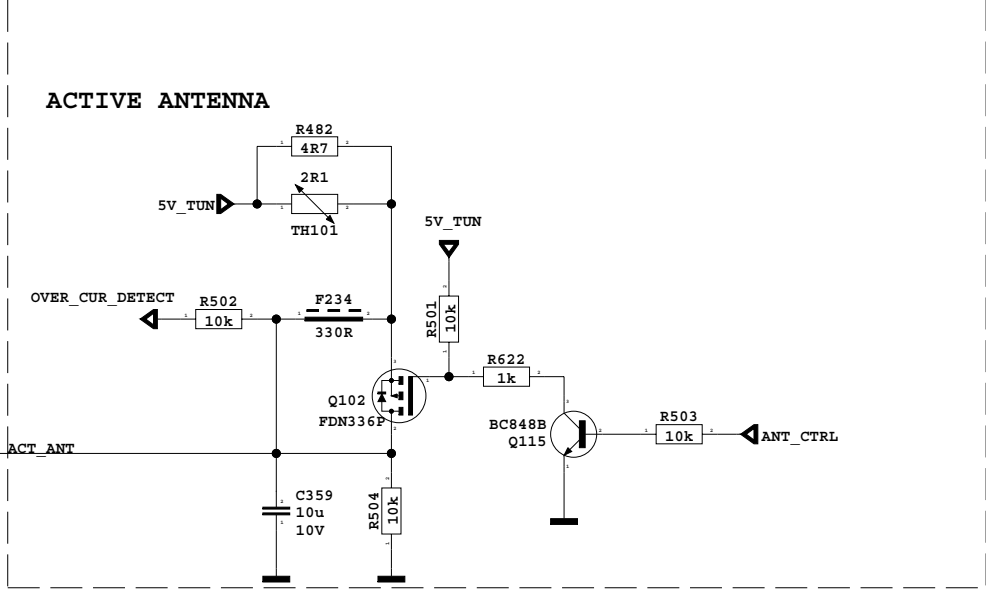
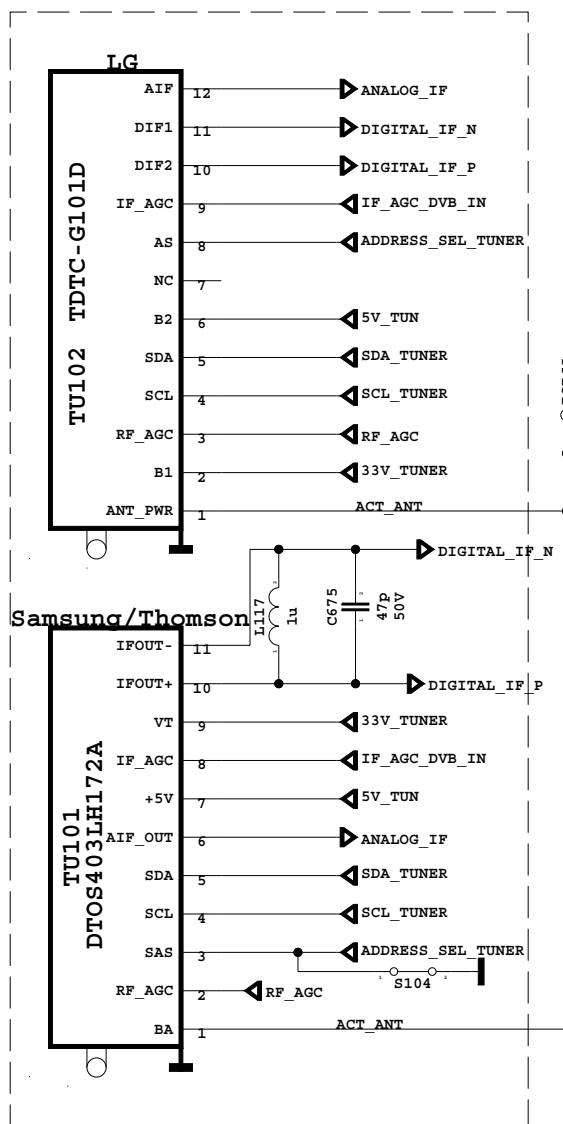


Notes:

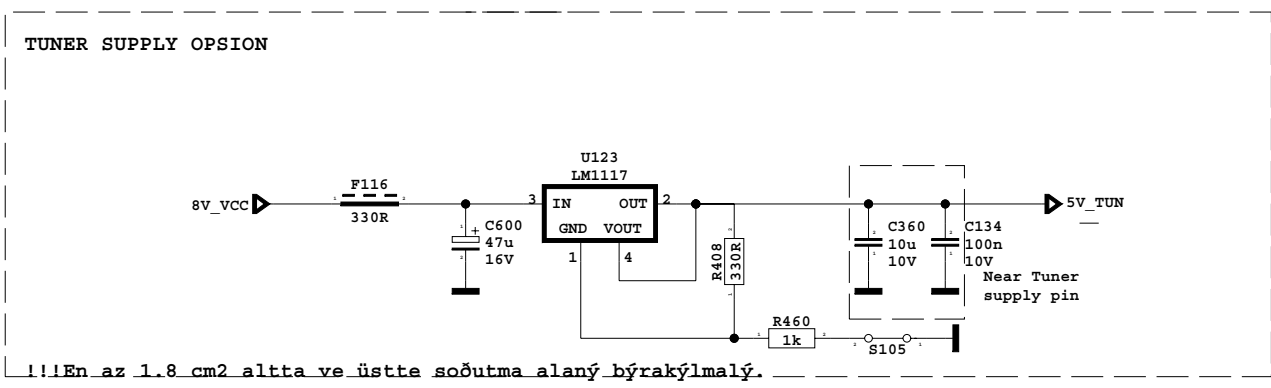
1. **APU:** Audio Processor Unit
2. **TSP:** Transport Stream Processor
3. **AIU:** Audio Interface Unit
4. **VDEC:** Video Decoder
5. **GPU:** Graphics Processing Unit
6. **EBI:** Extended Bus Interface

12.3 MSTAR Block Diagram

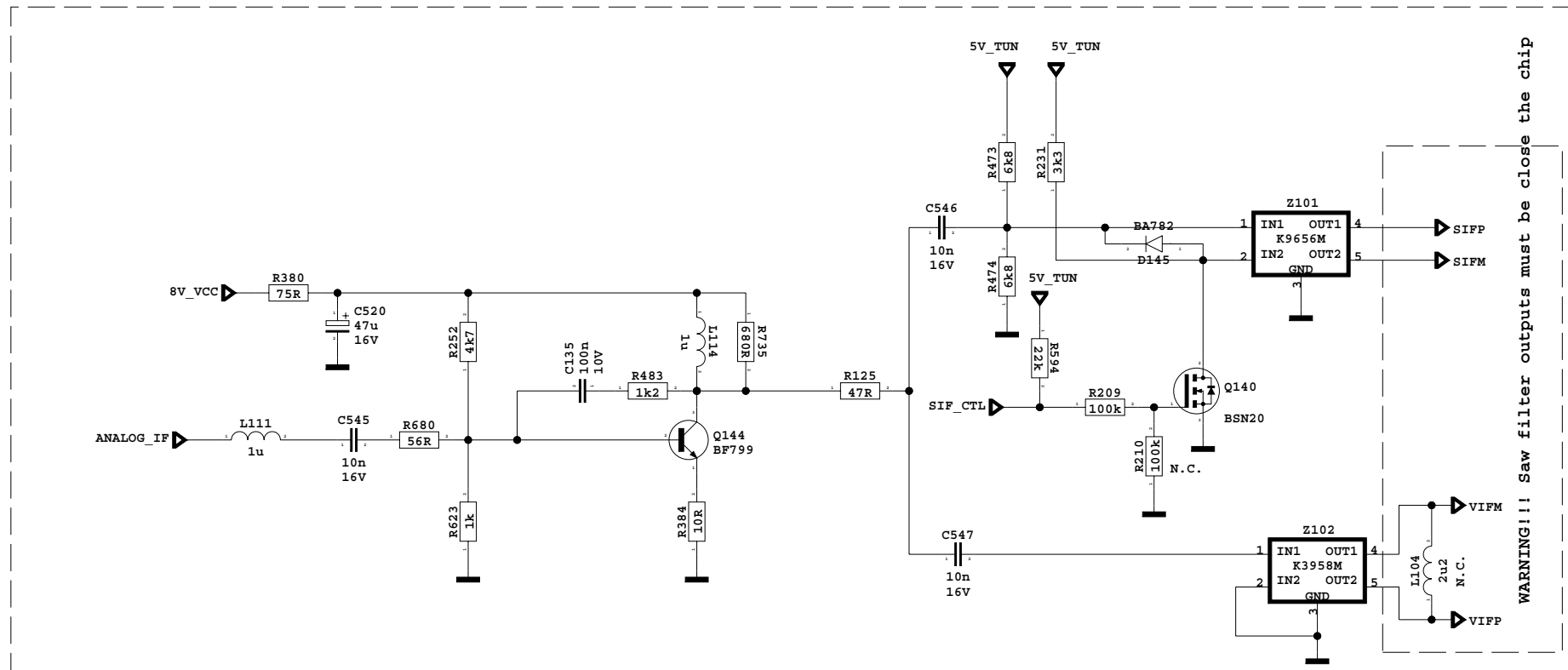
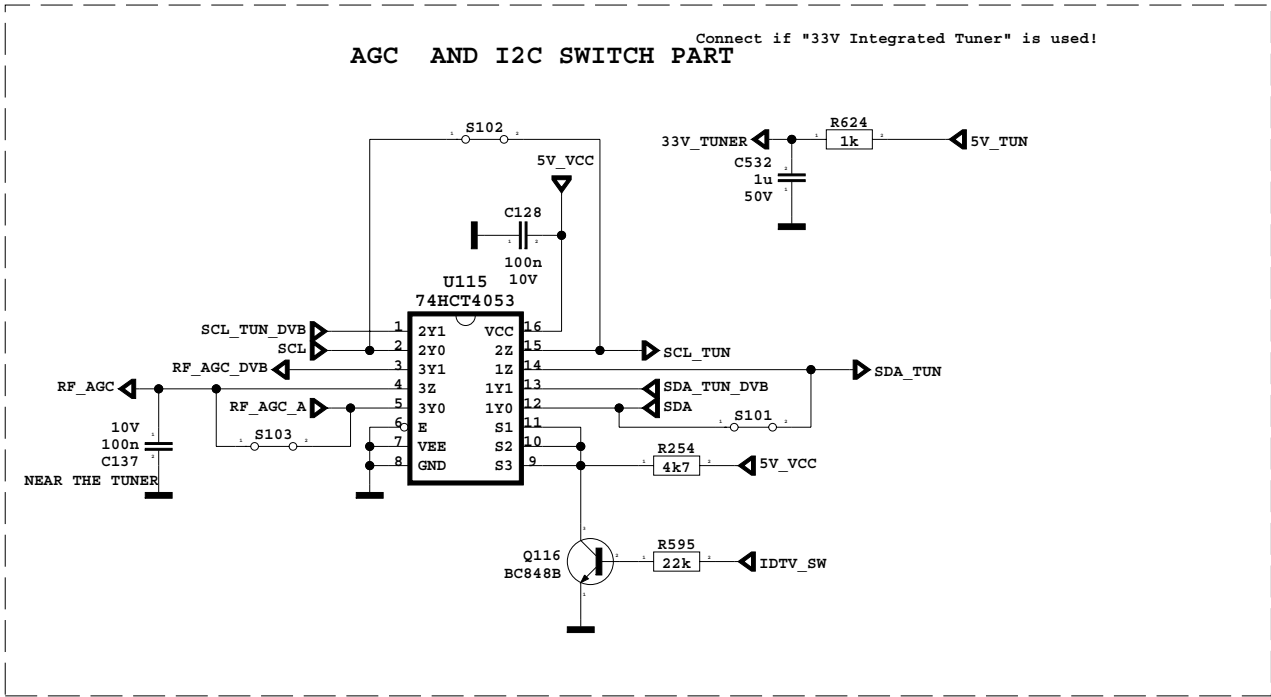




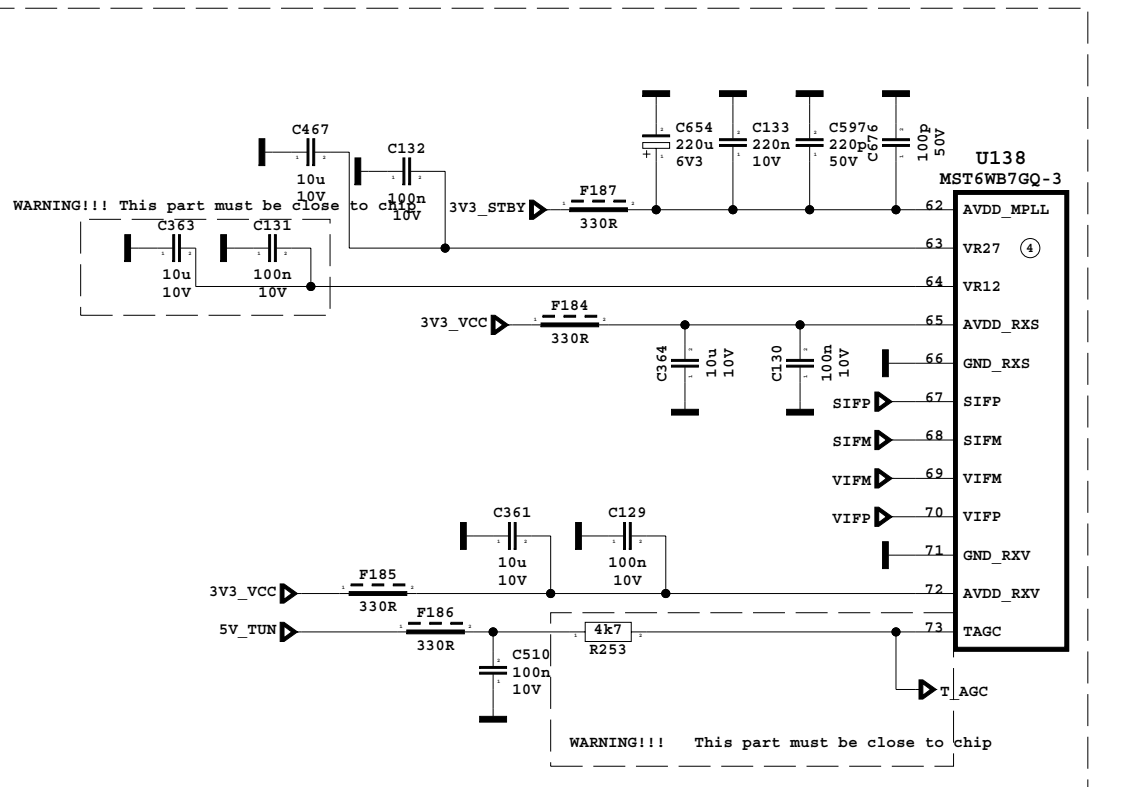
This part must be placed near the tuner

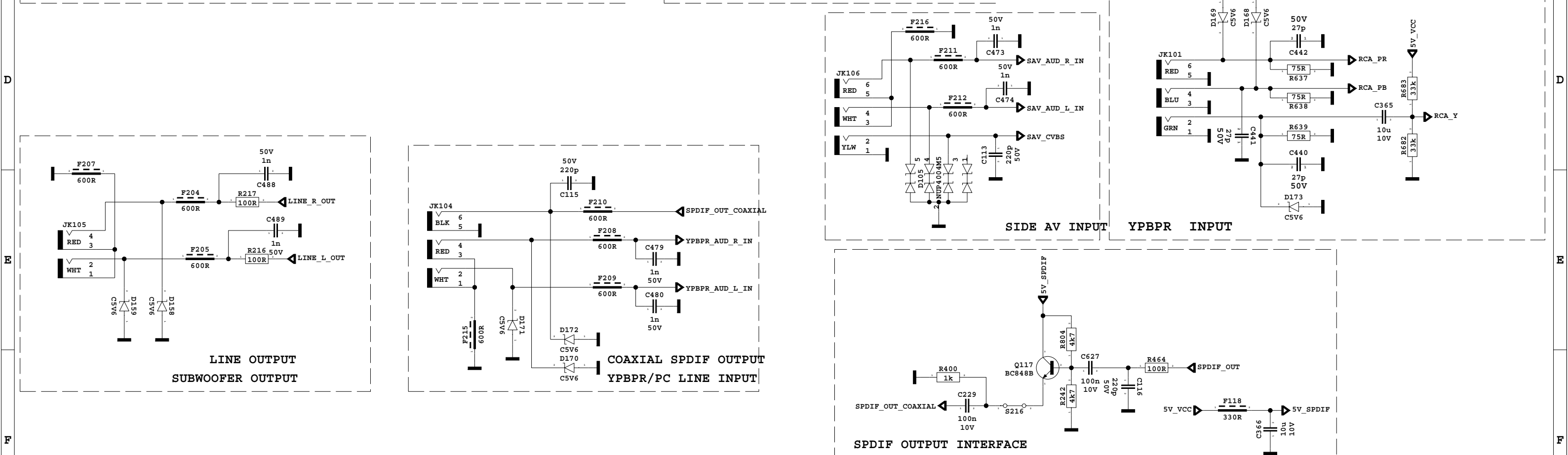
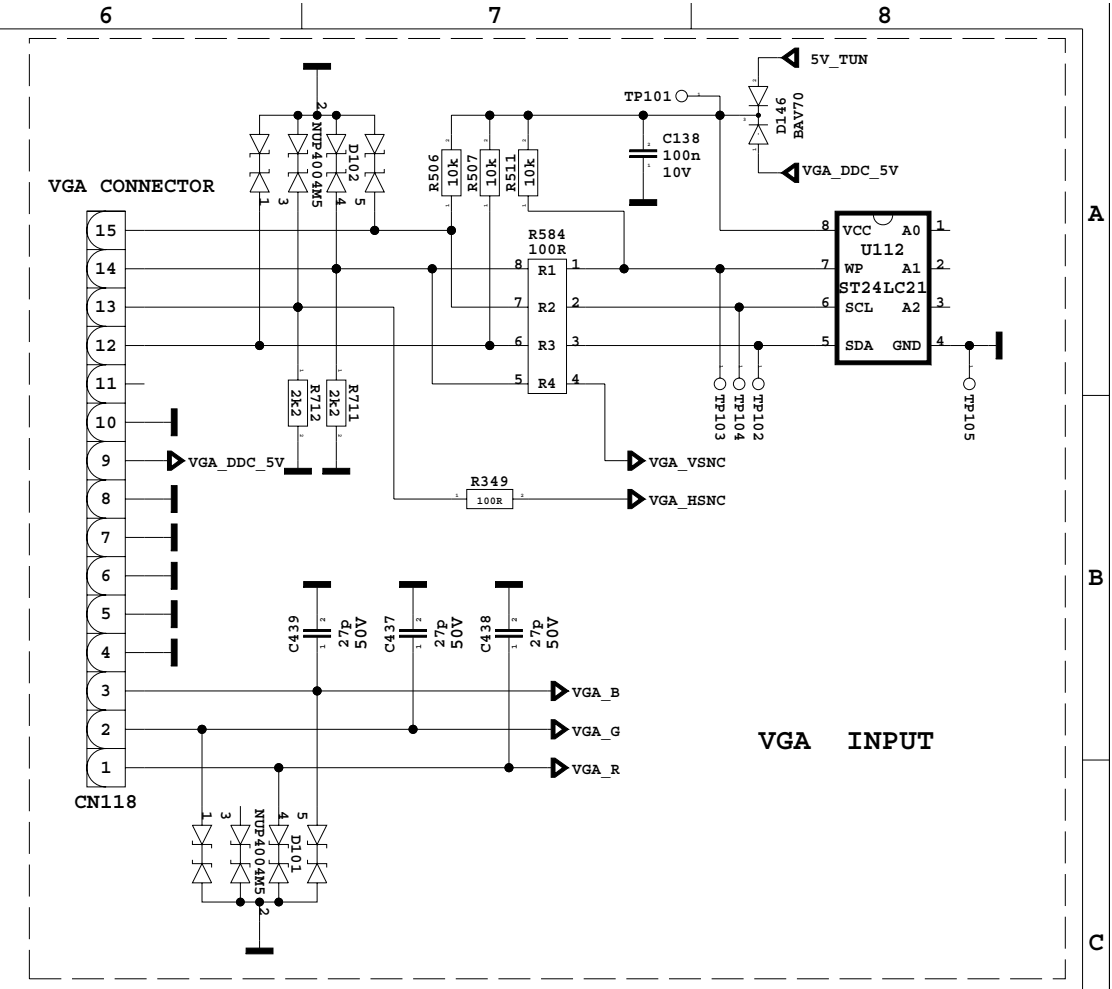
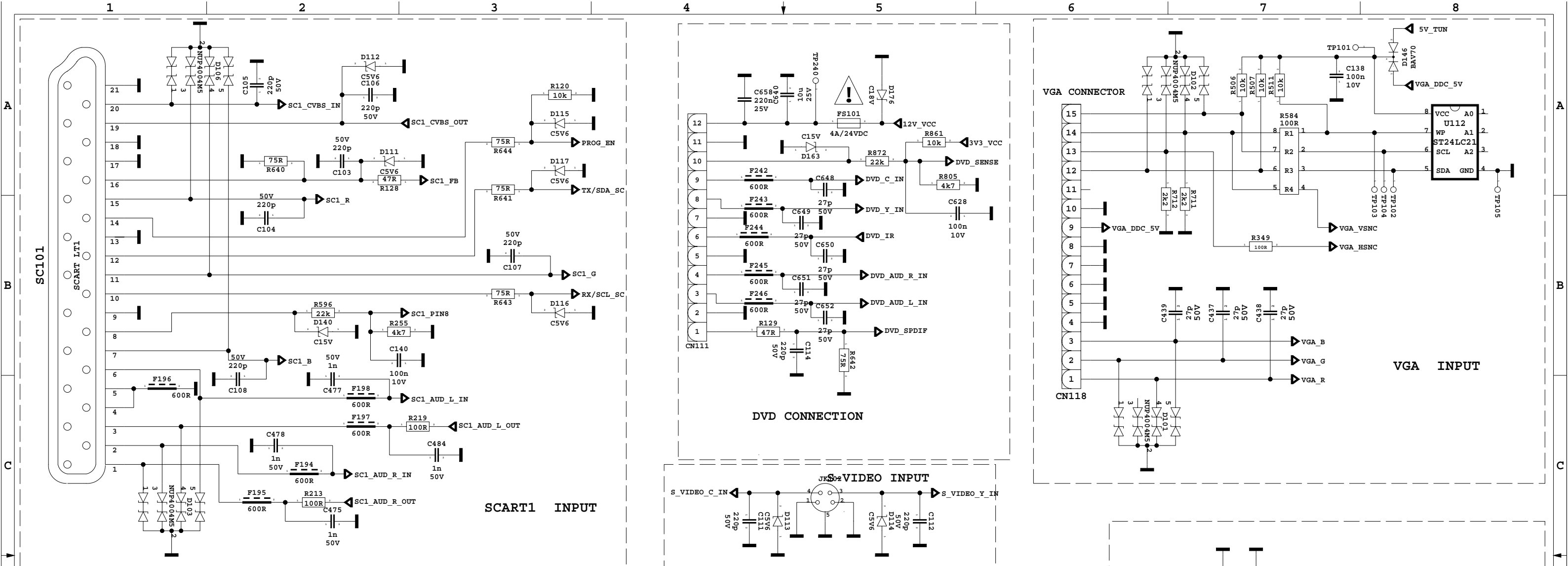


!!!En az 1.8 cm2 altta ve üstte sođutma alanı byrakılmaly.

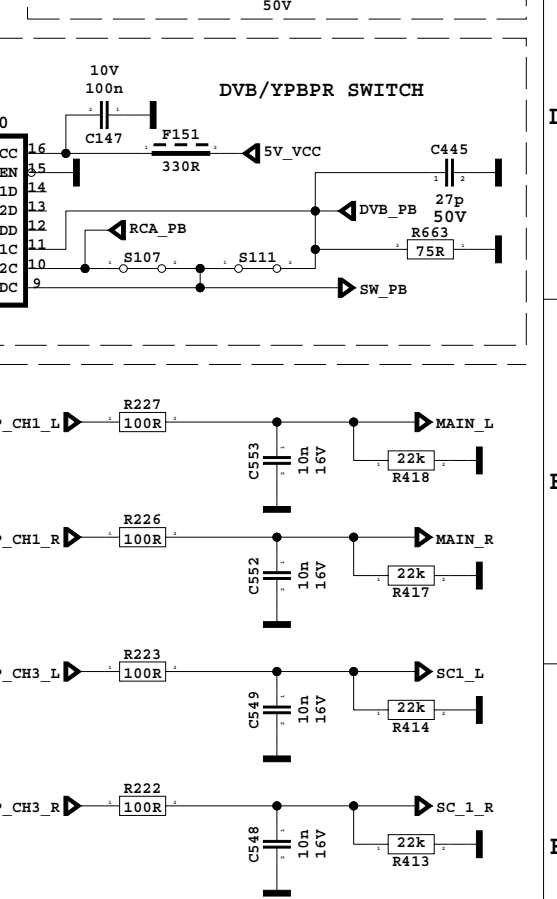
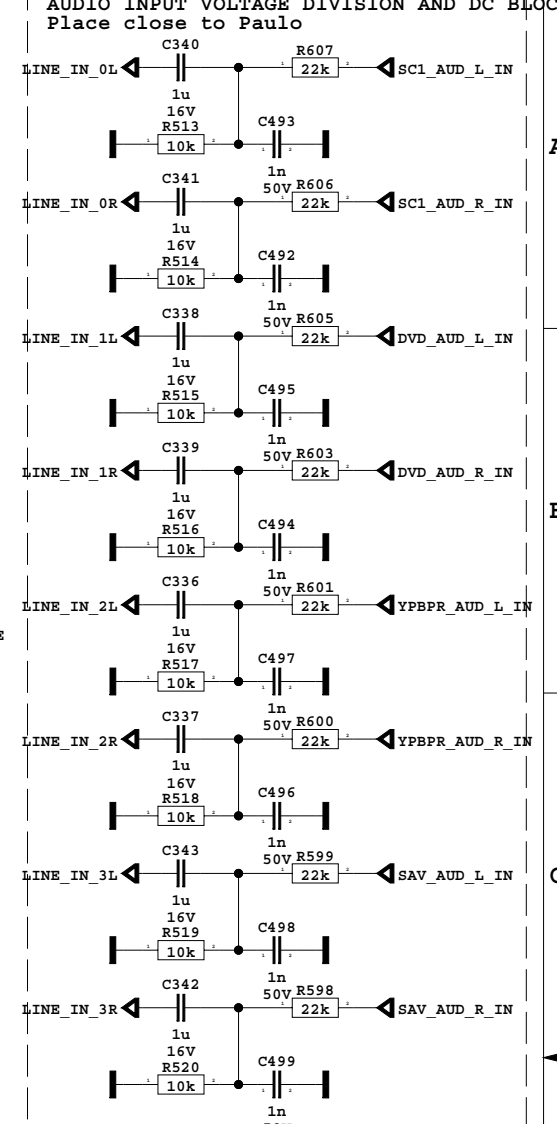
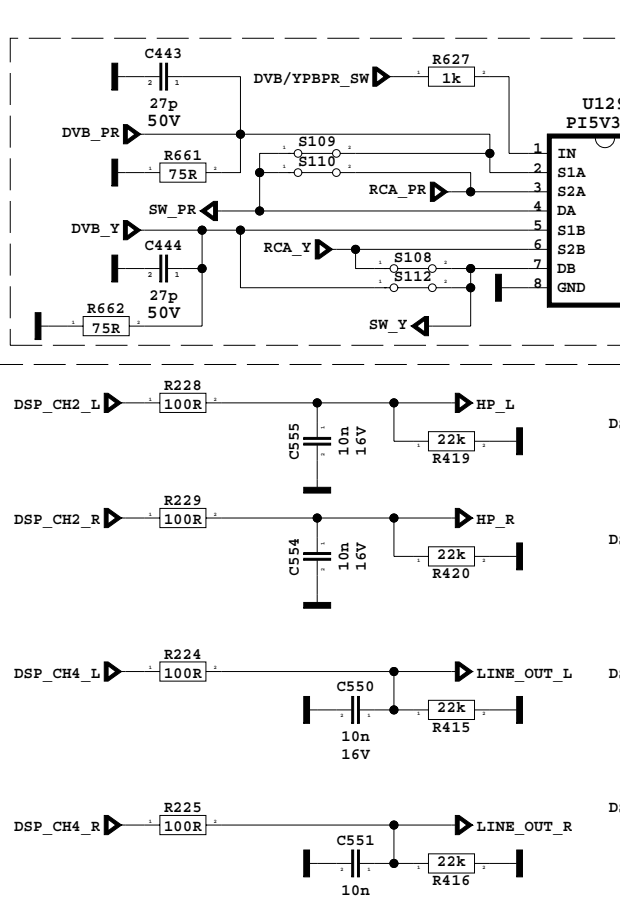
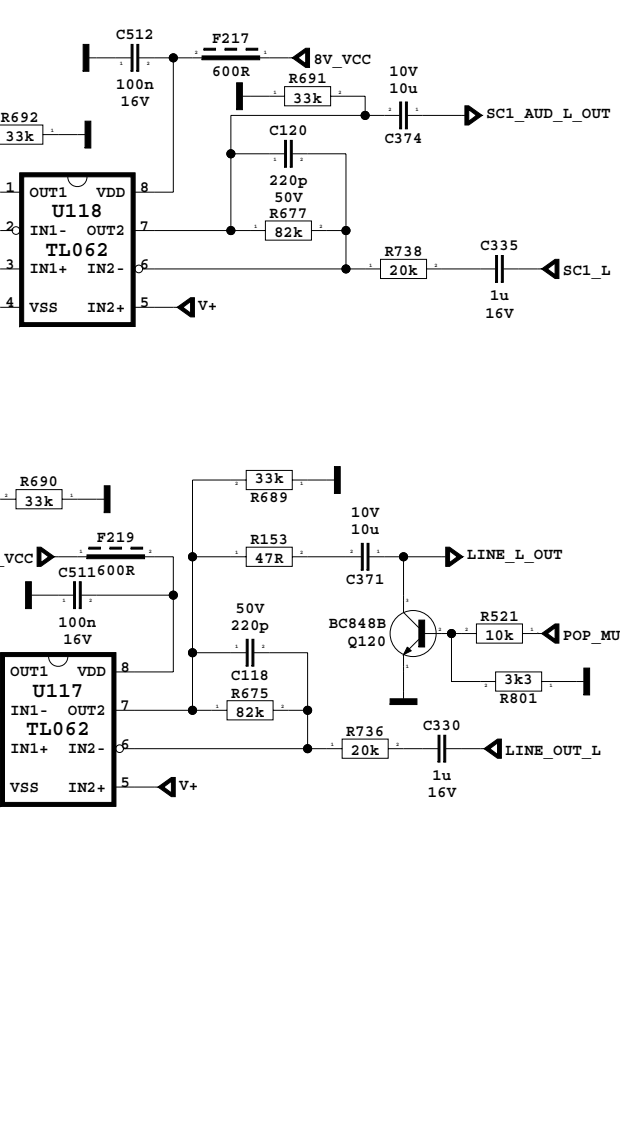
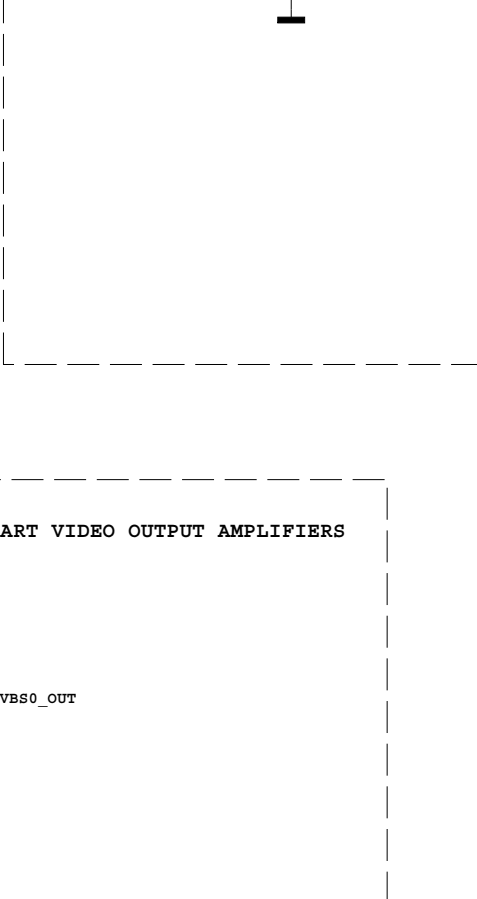
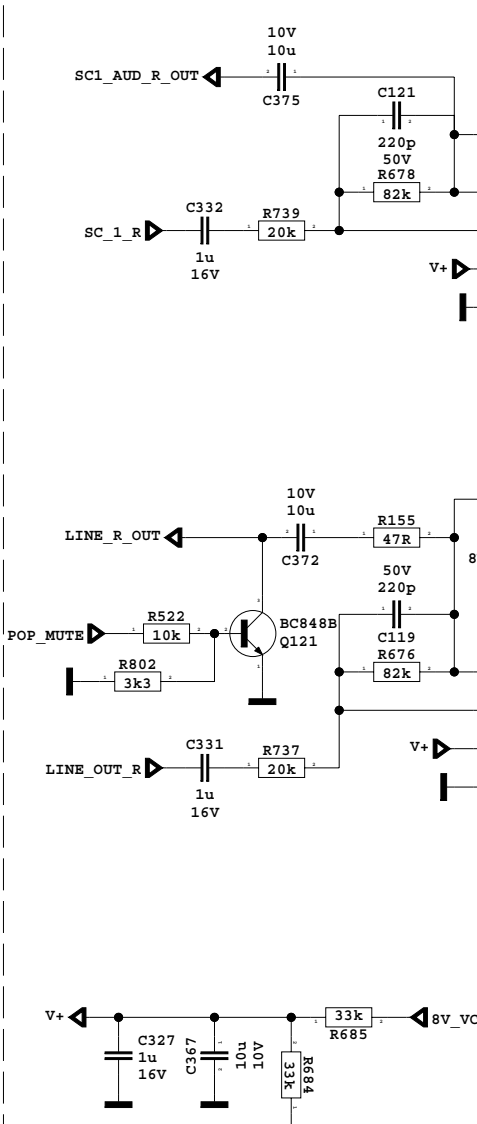
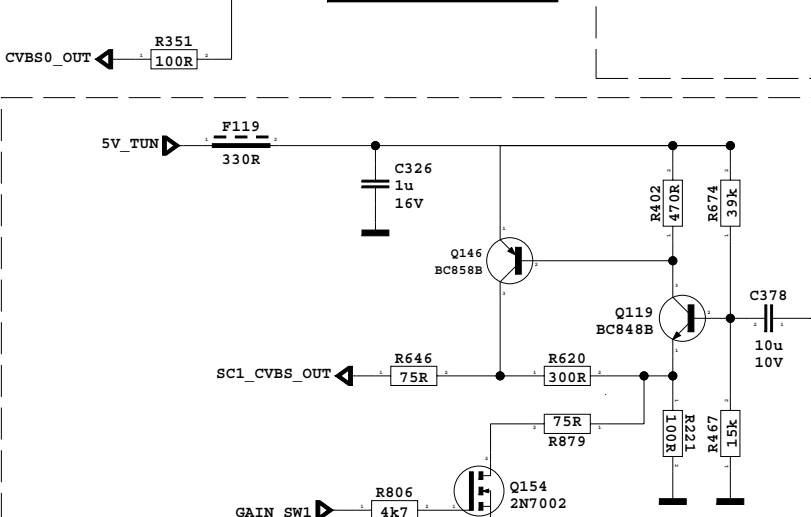
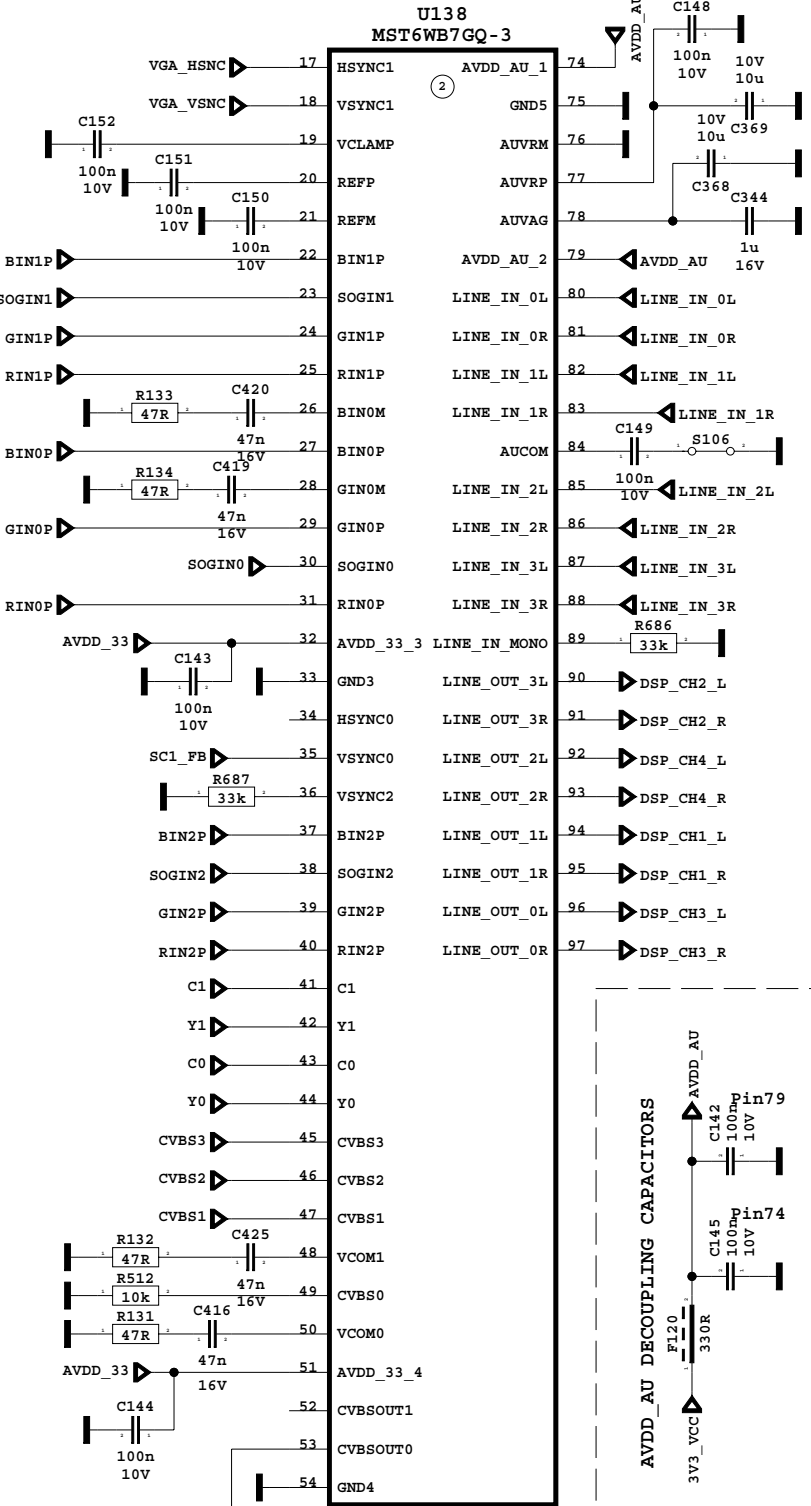
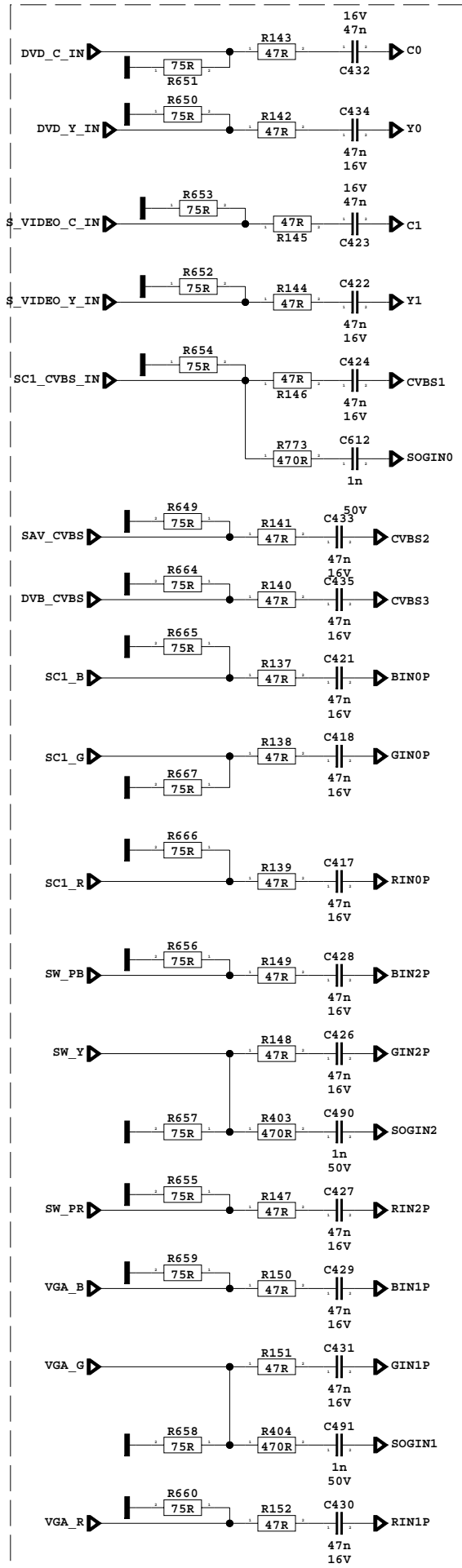


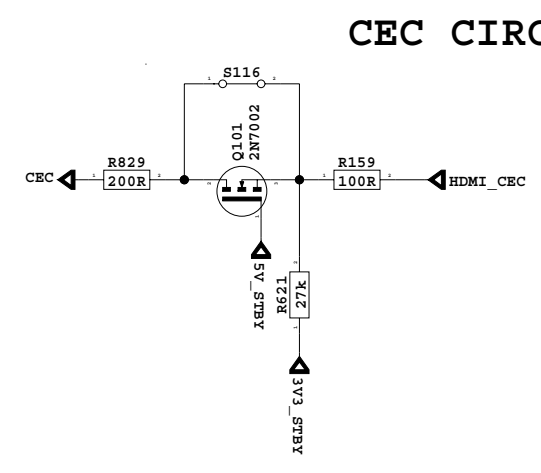
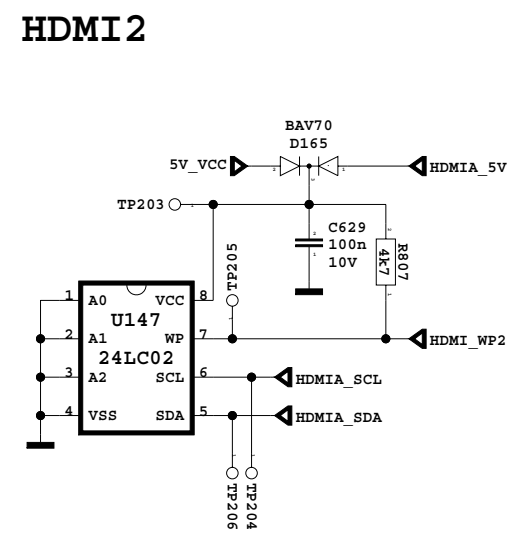
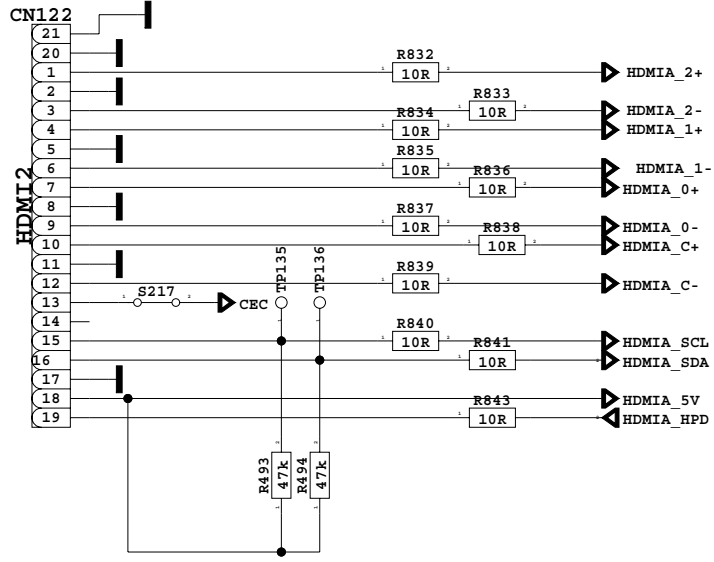
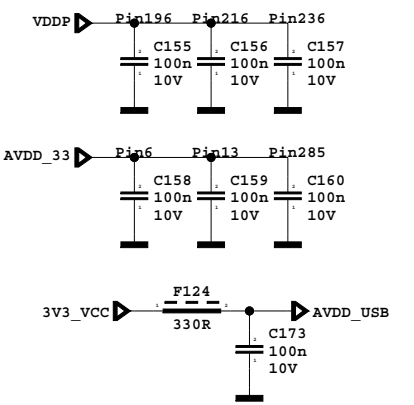
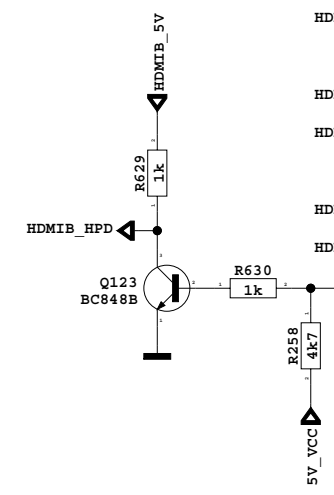
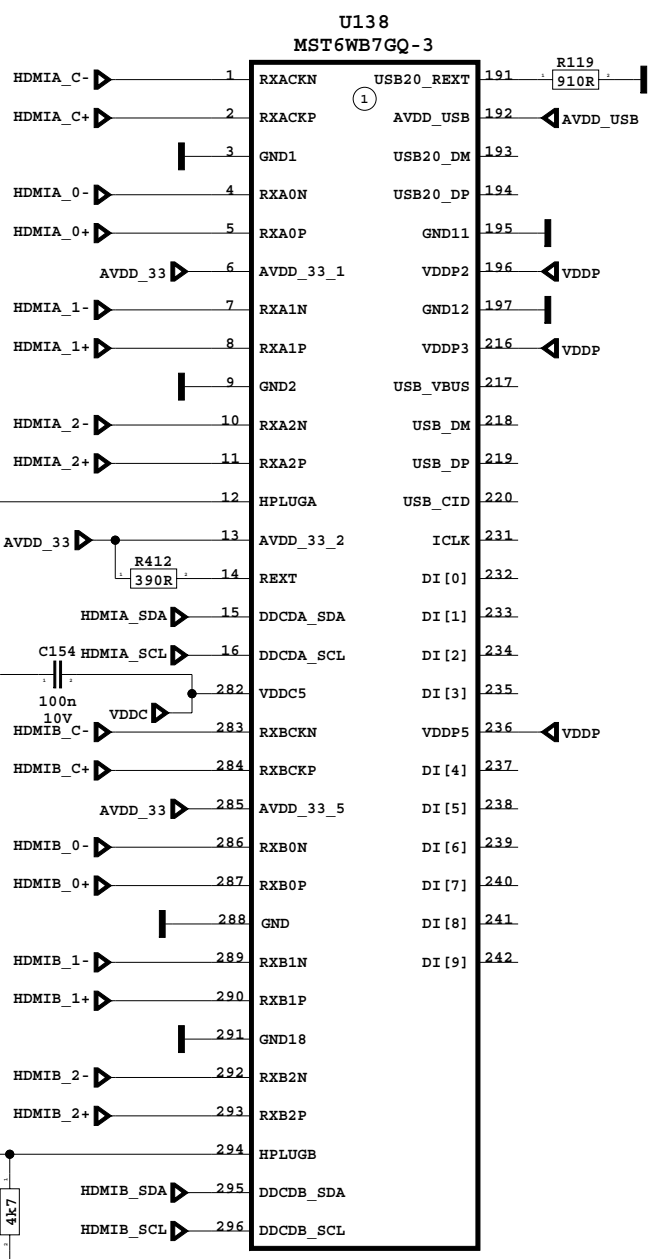
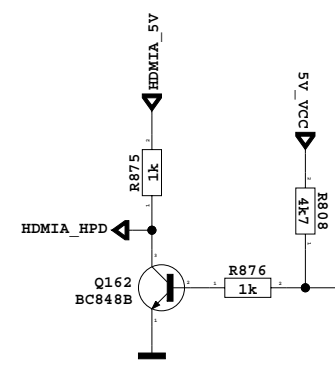
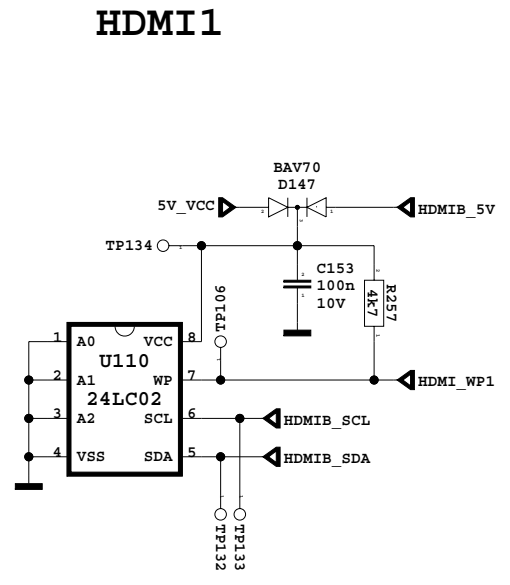
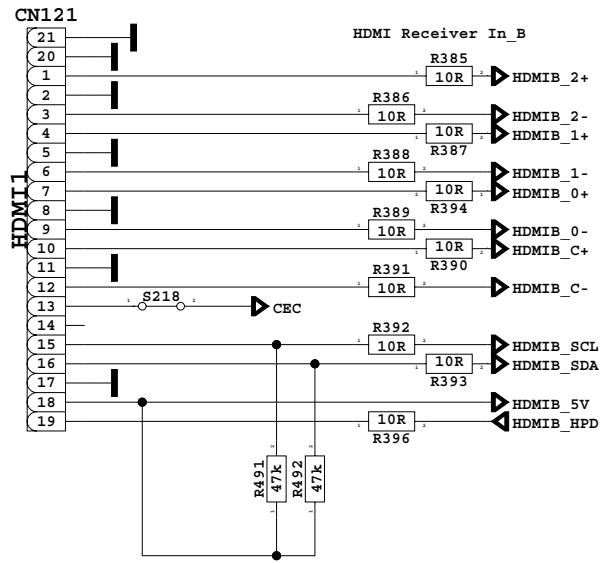
WARNING!!! Saw filter outputs must be close the chip





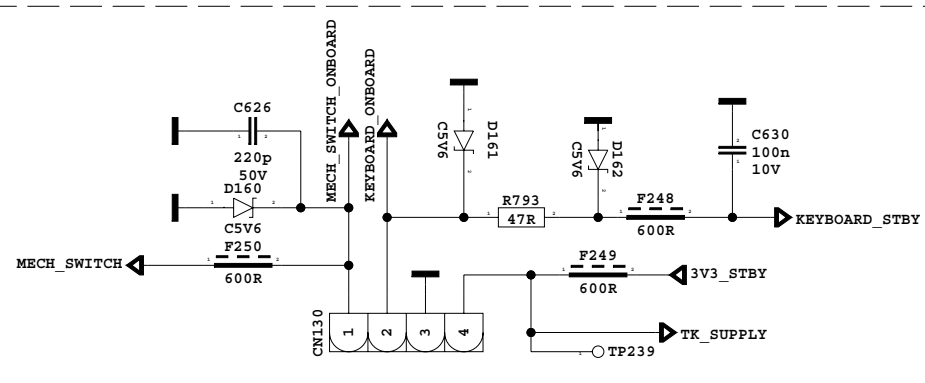
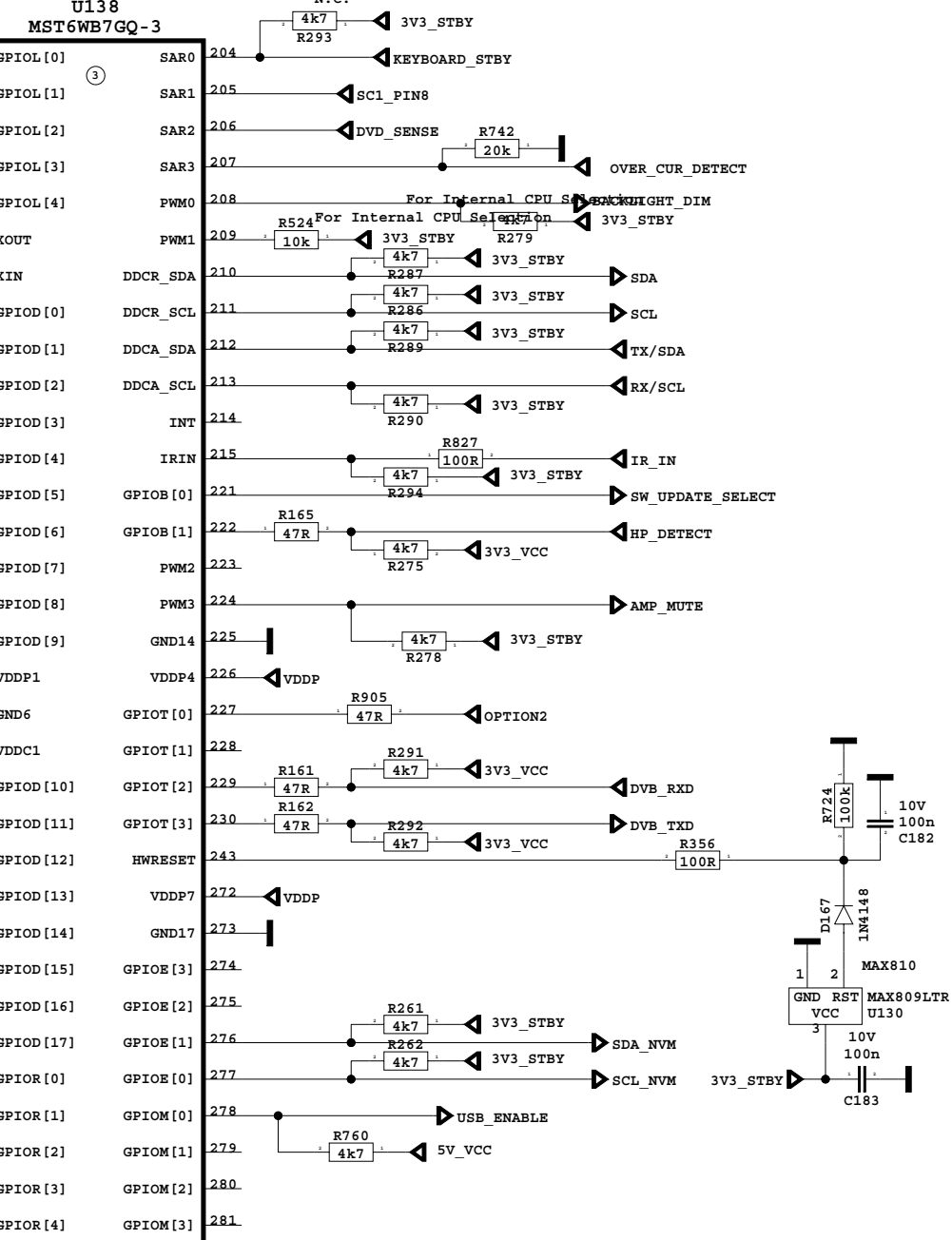
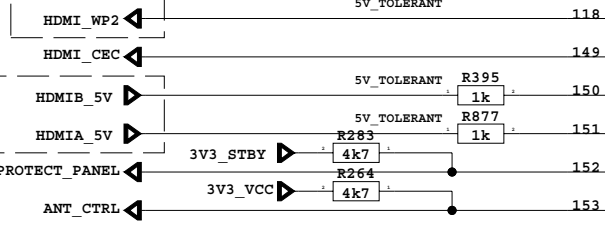
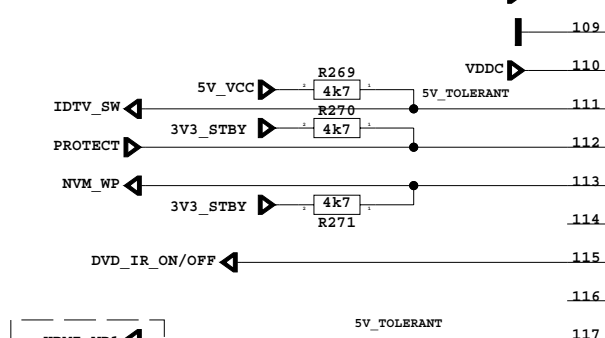
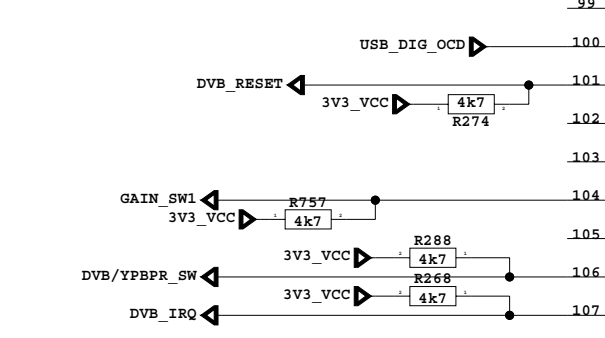
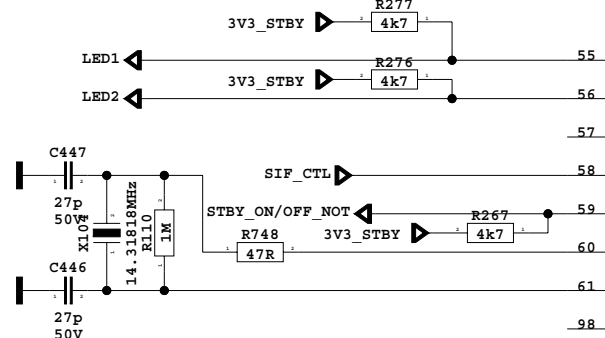
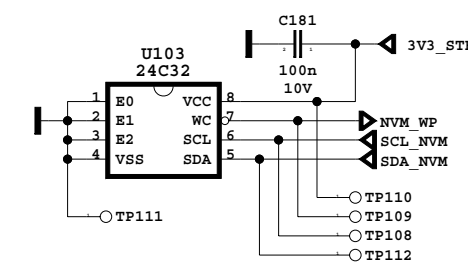
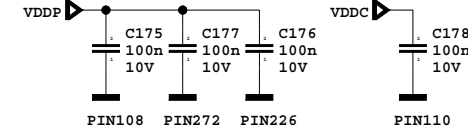
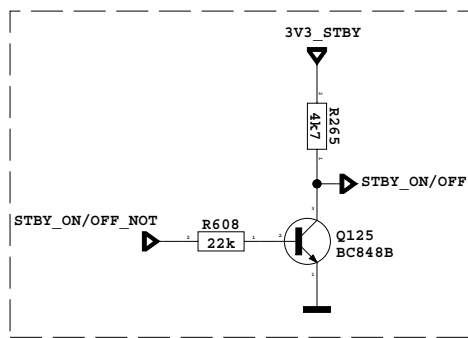
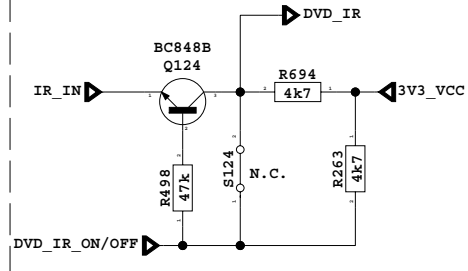
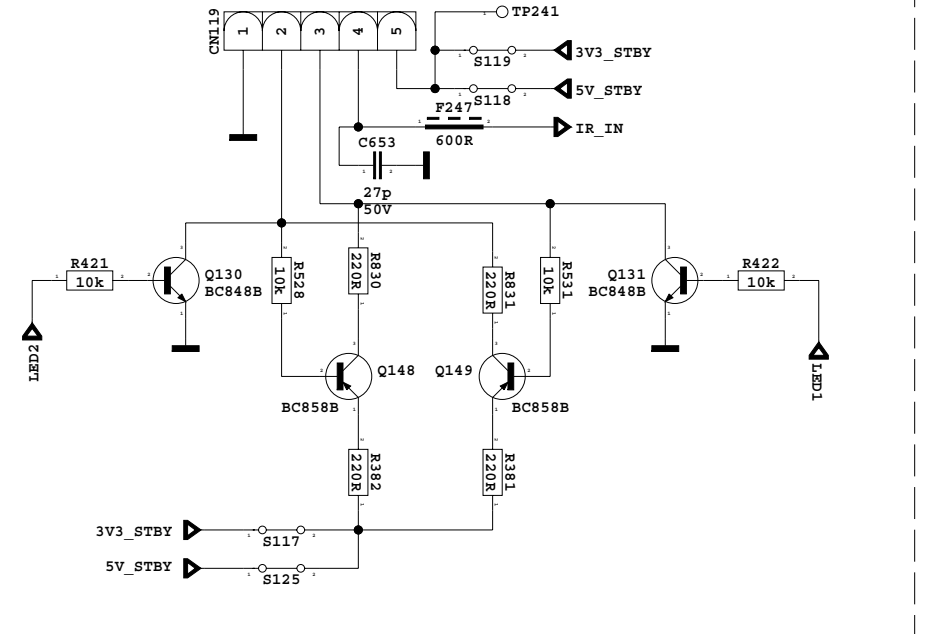
VIDEO TERMINATIONS AND DIFFERENTIAL TRACING
Place 75R termination resistors close to Paulo reference GNDs



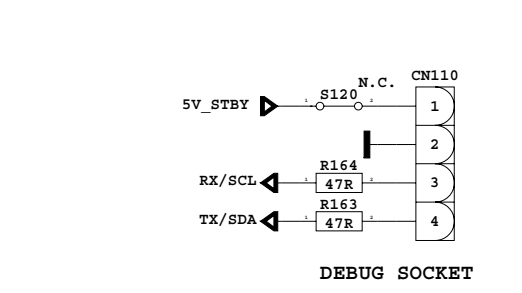
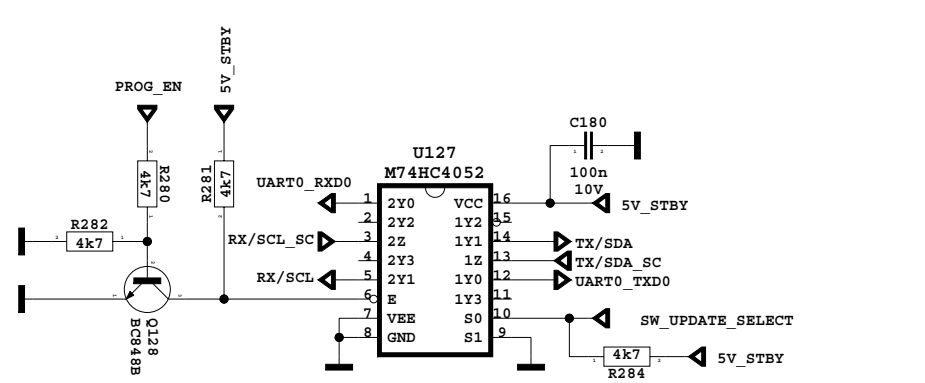


CEC CIRCUIT

LED

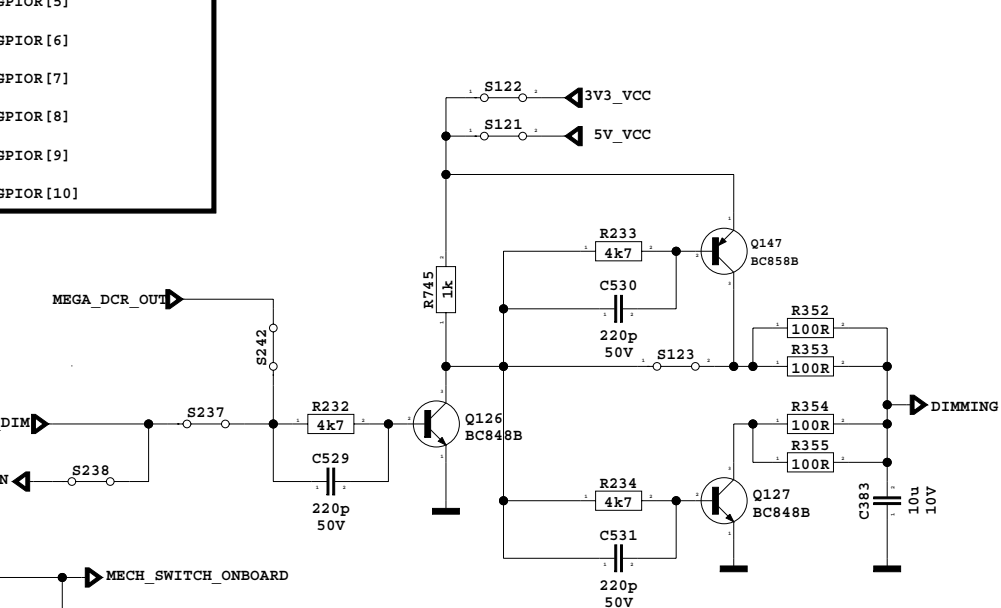
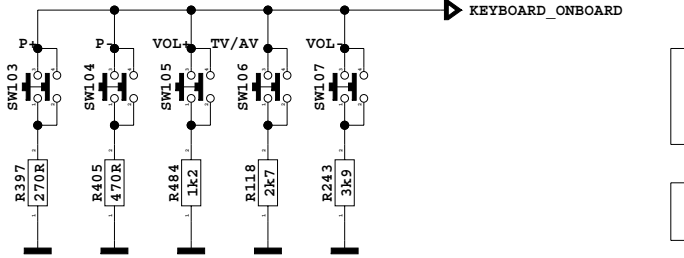


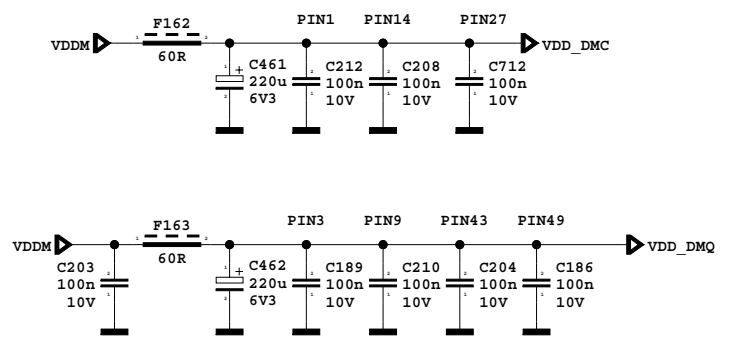
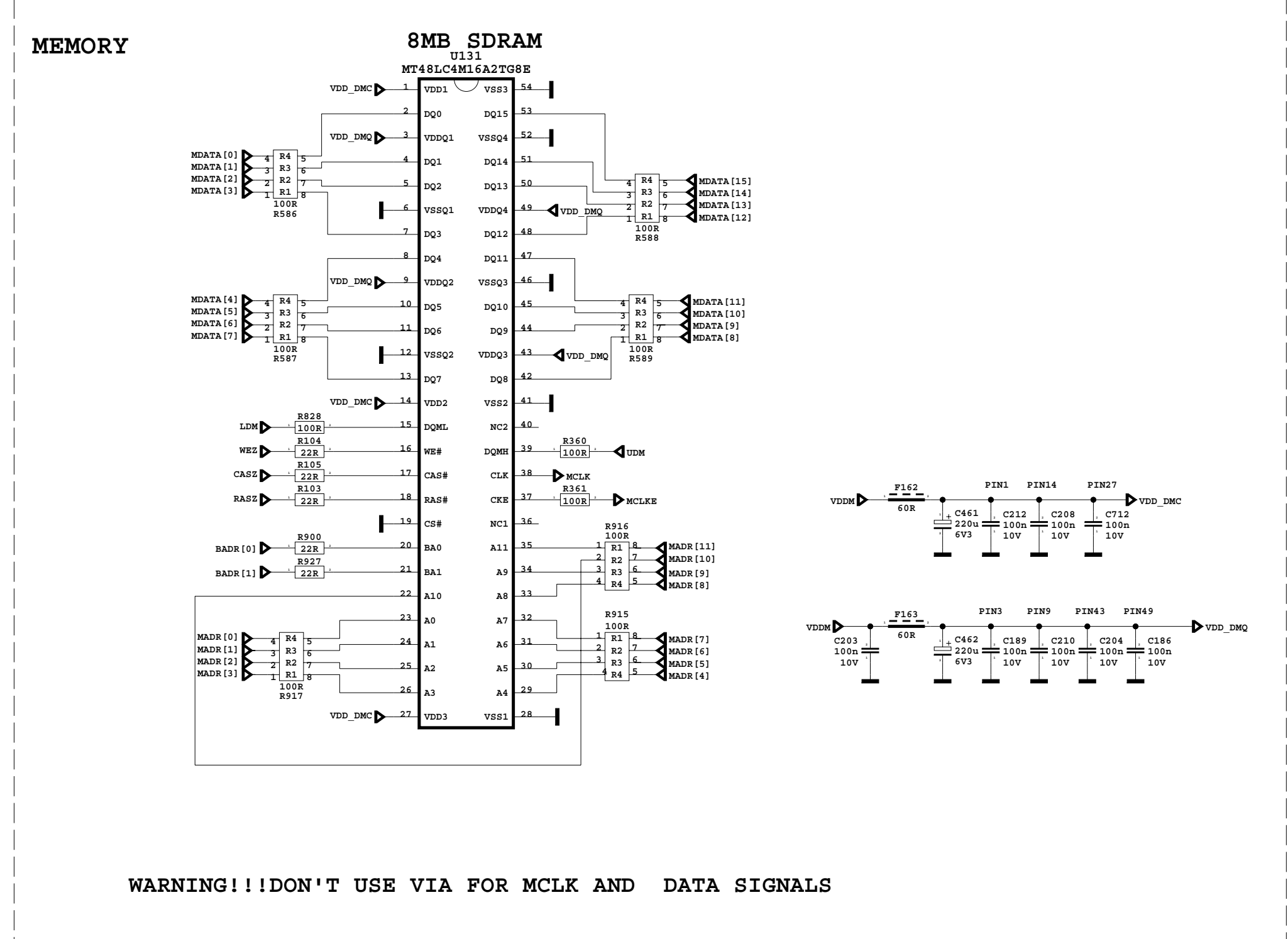
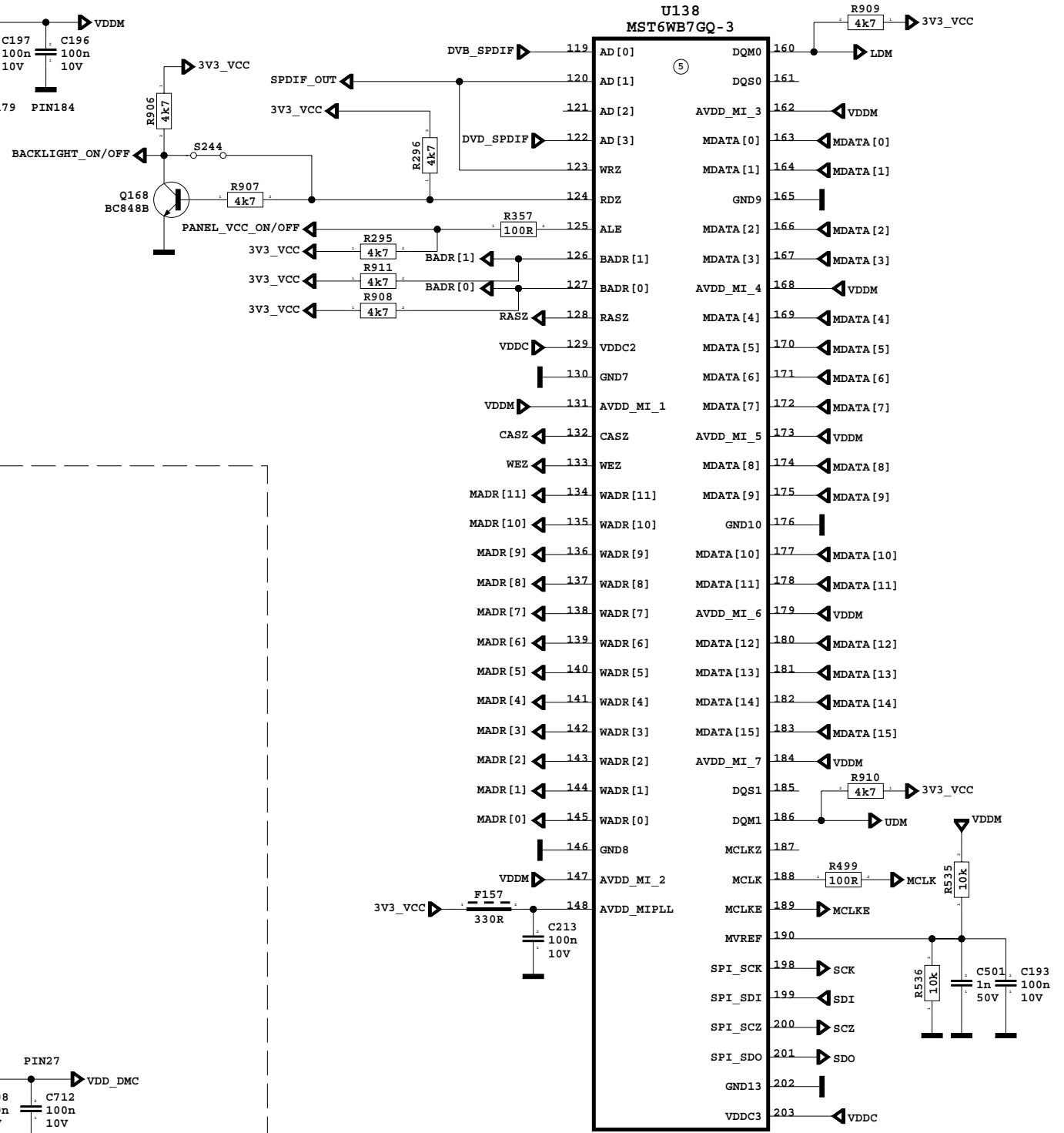
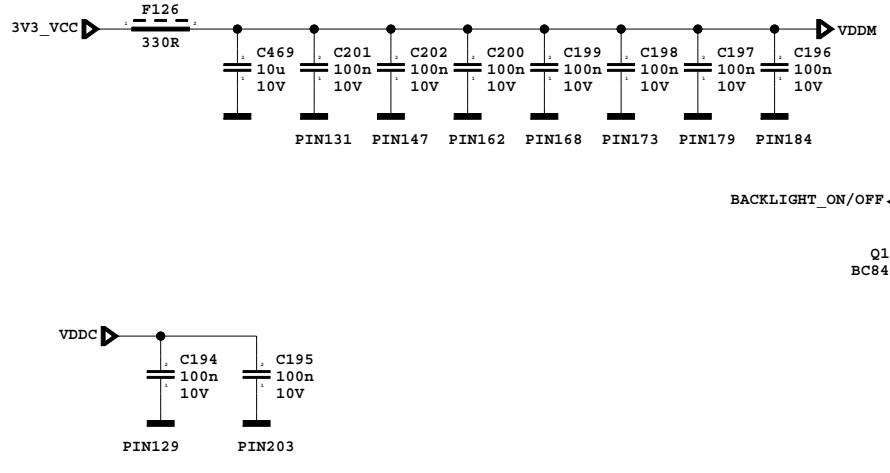
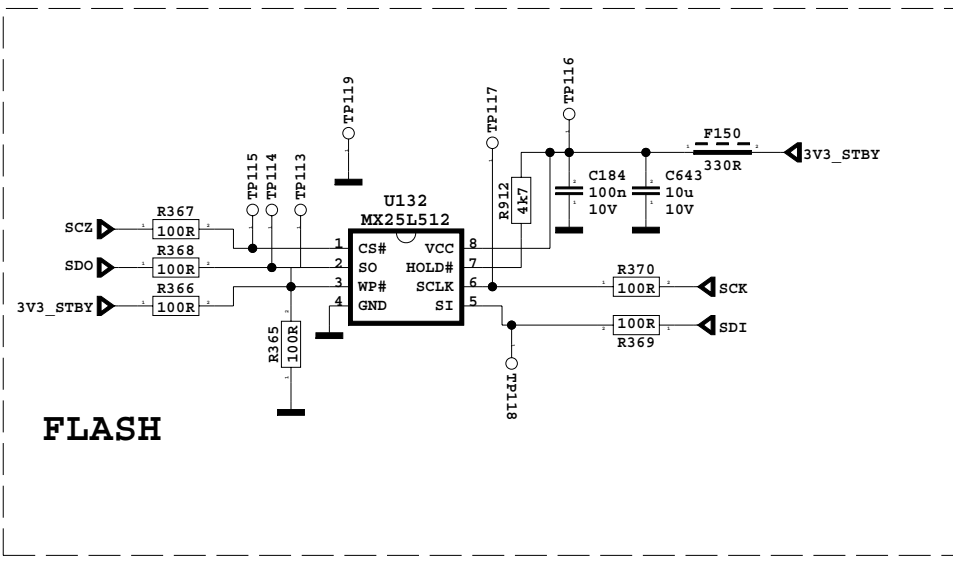
PROGRAMMING PART



PROG_EN	
0	HC4052 DISABLE
1	HC4052 ENABLE
SW_UPDATE_SELECT	
0	DVB_SW_UPDATE
1	ANALOG_SW_UPDATE

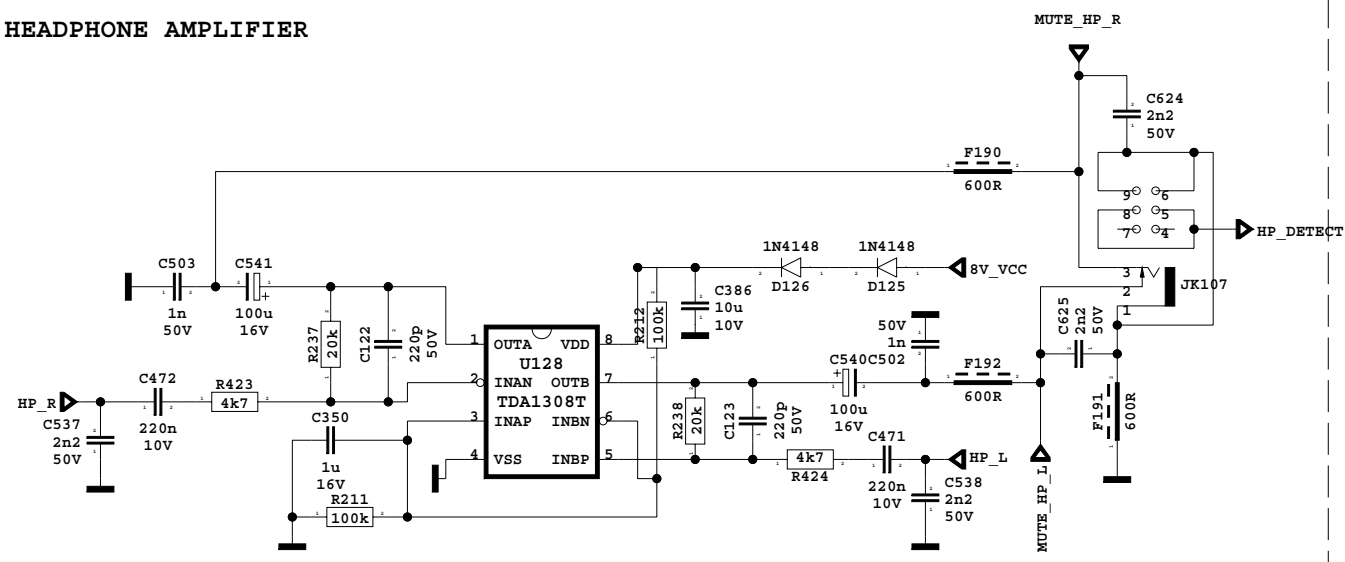
PUSH V+ AND V- AT THE SAME TIME FOR MENU



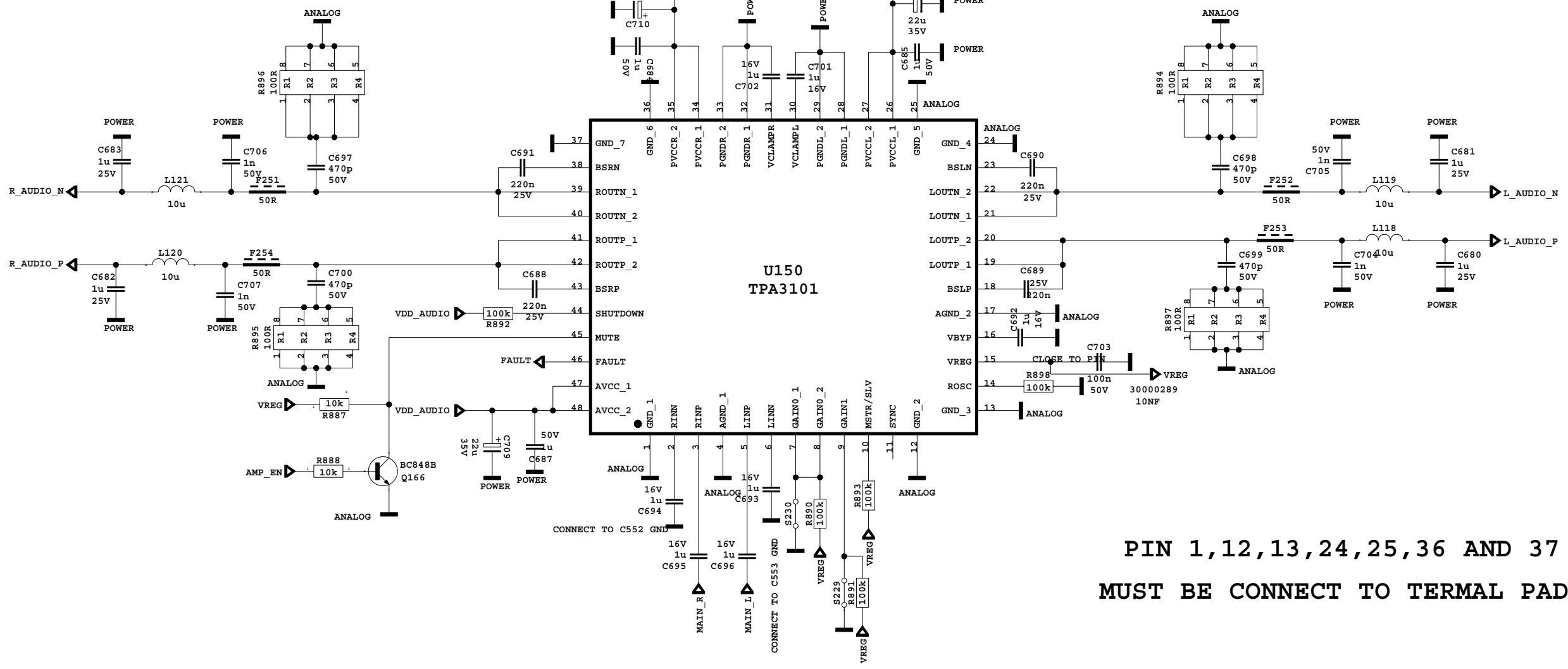
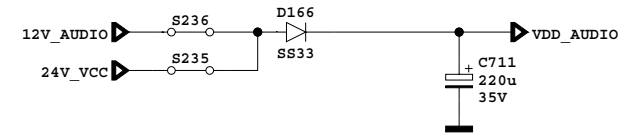
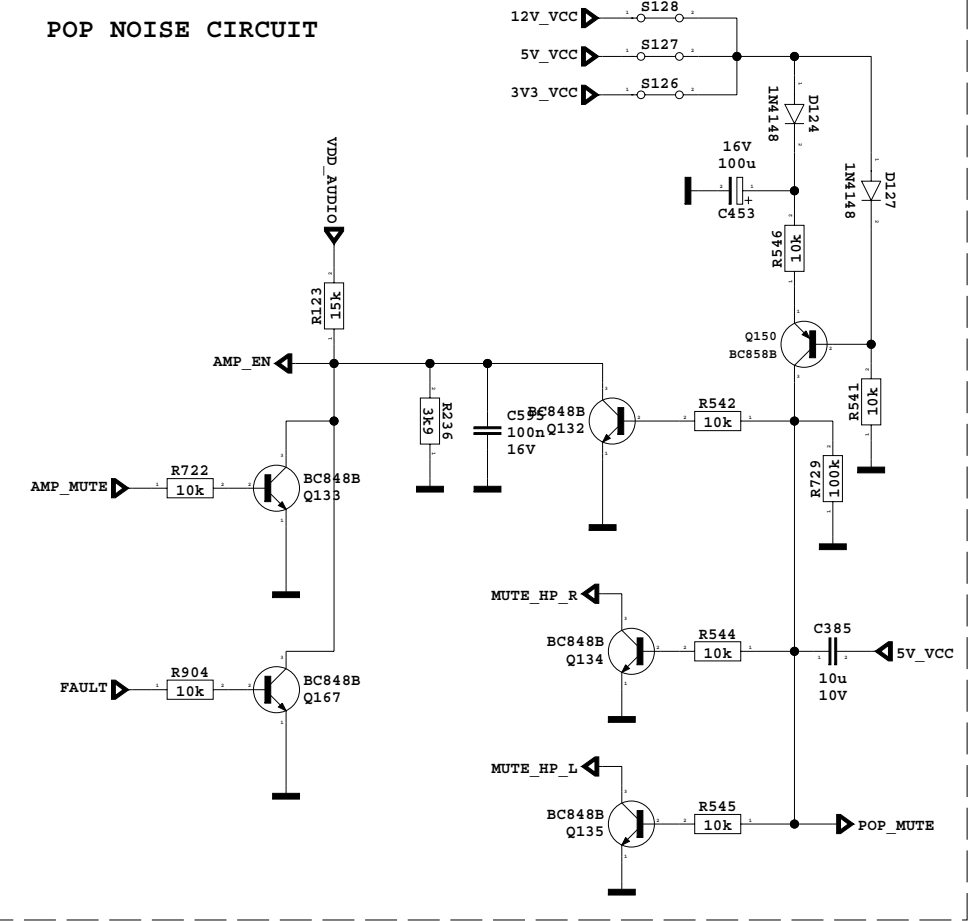


WARNING!!!DON'T USE VIA FOR MCLK AND DATA SIGNALS

HEADPHONE AMPLIFIER

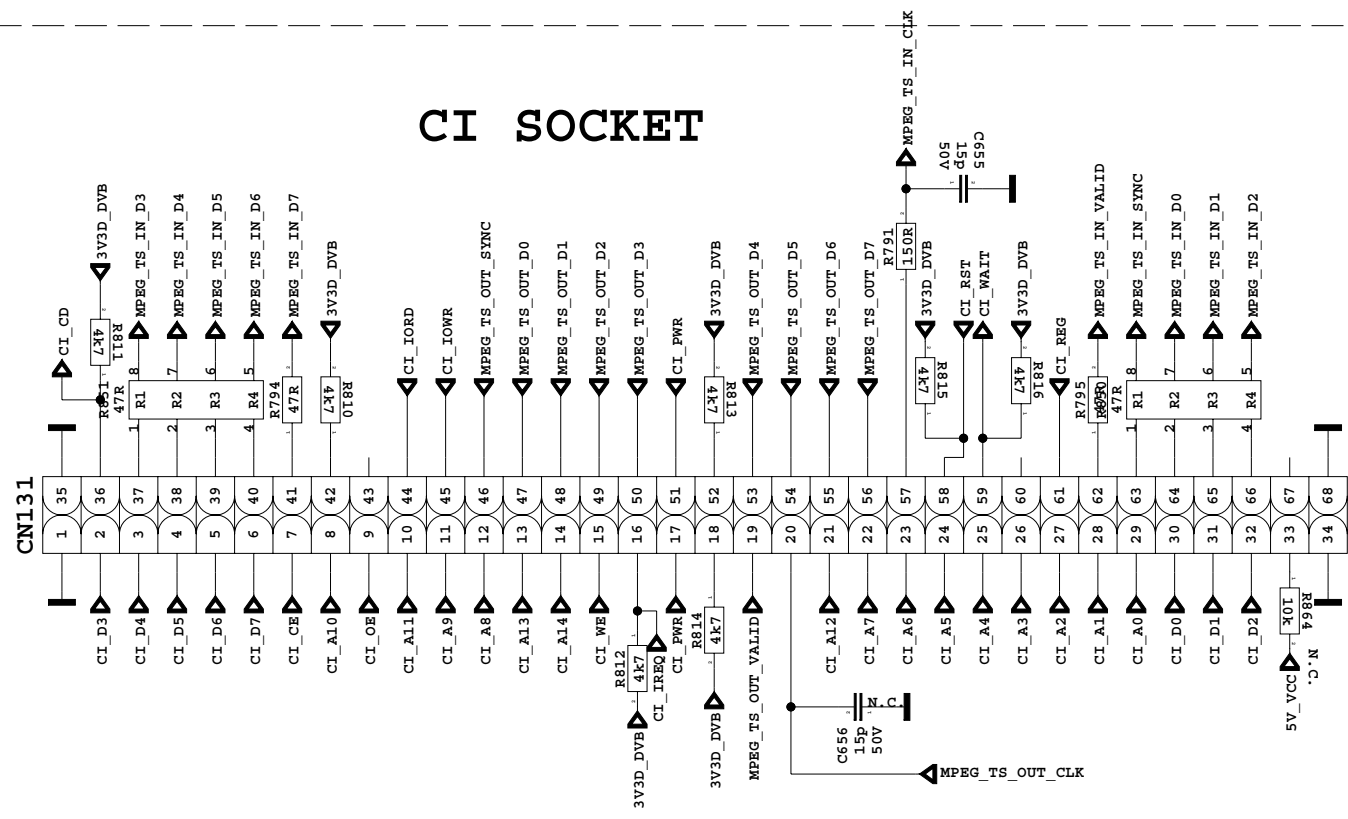


POP NOISE CIRCUIT

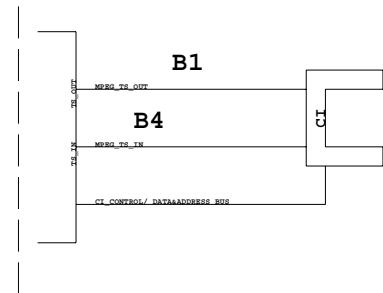


PIN 1,12,13,24,25,36 AND 37
MUST BE CONNECT TO TERMAL PAD

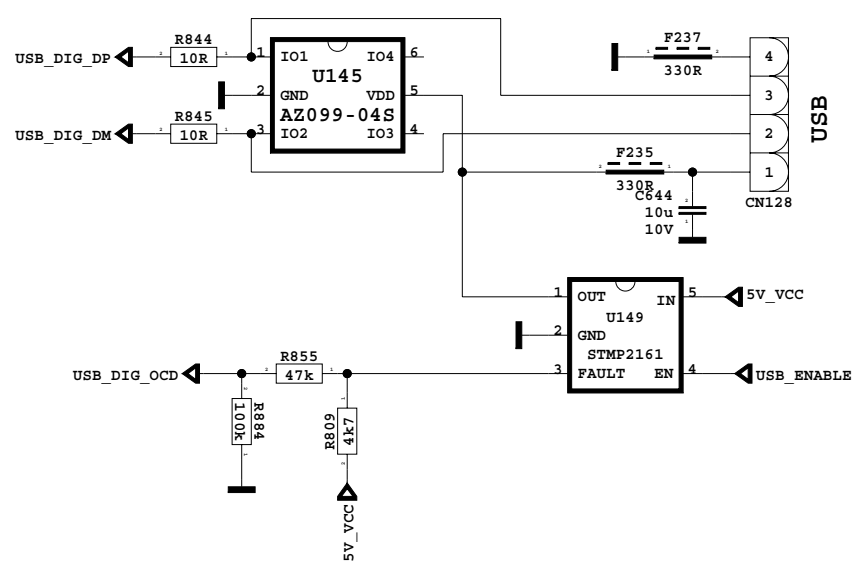
CI SOCKET



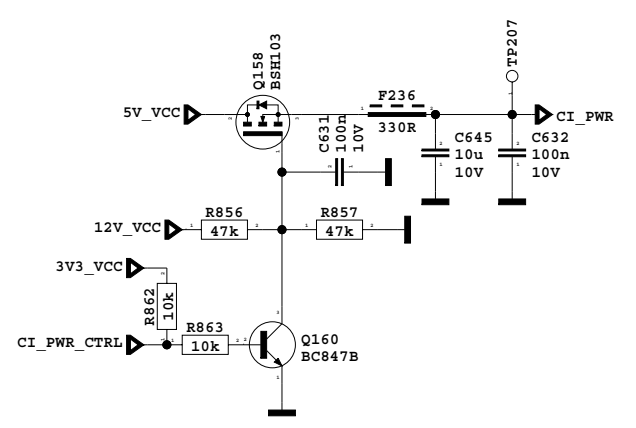
TS ROUTING



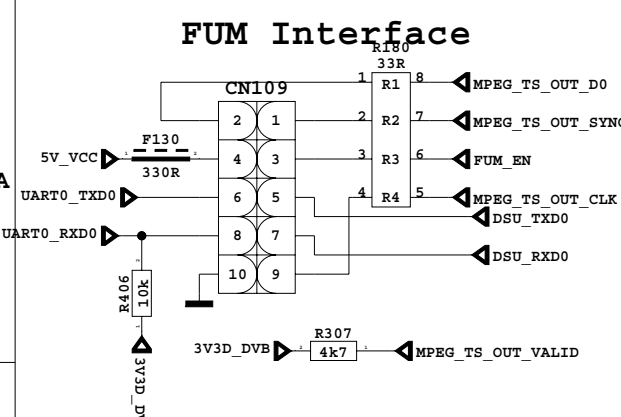
USB INTERFACE



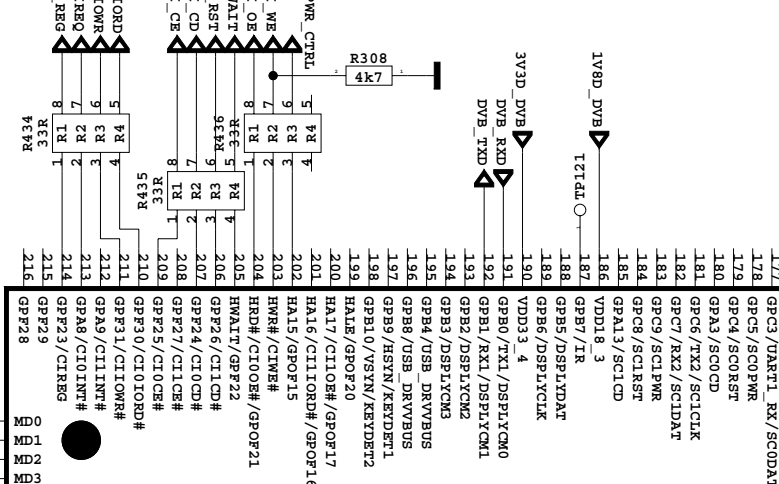
CI 5V SWITCH CIRCUIT



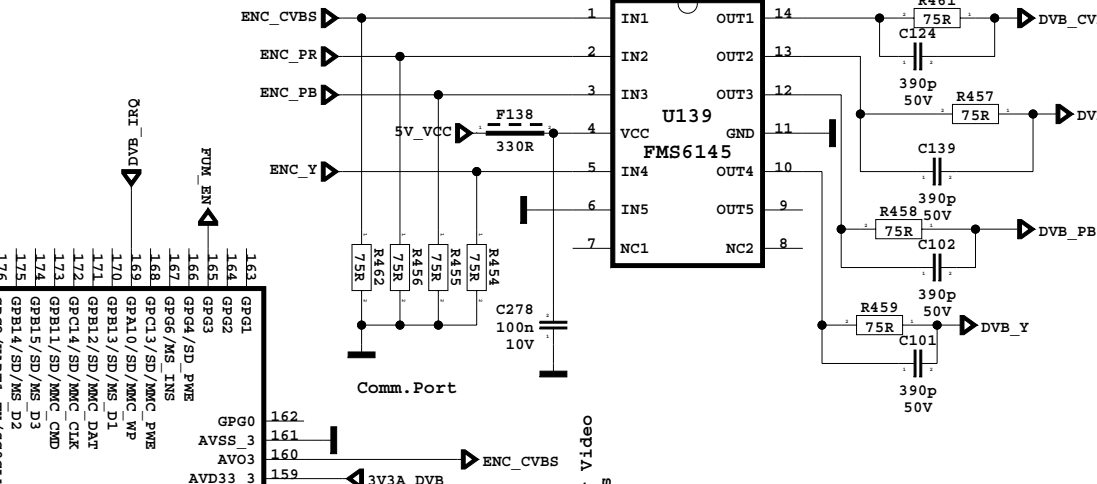
FUM Interface



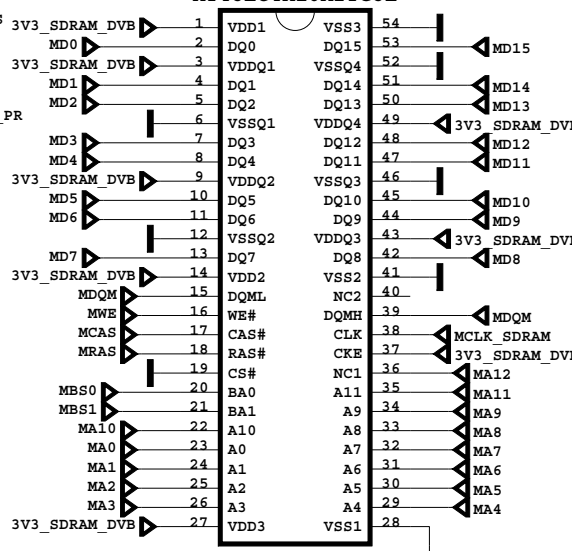
CONTROL SIGNALS



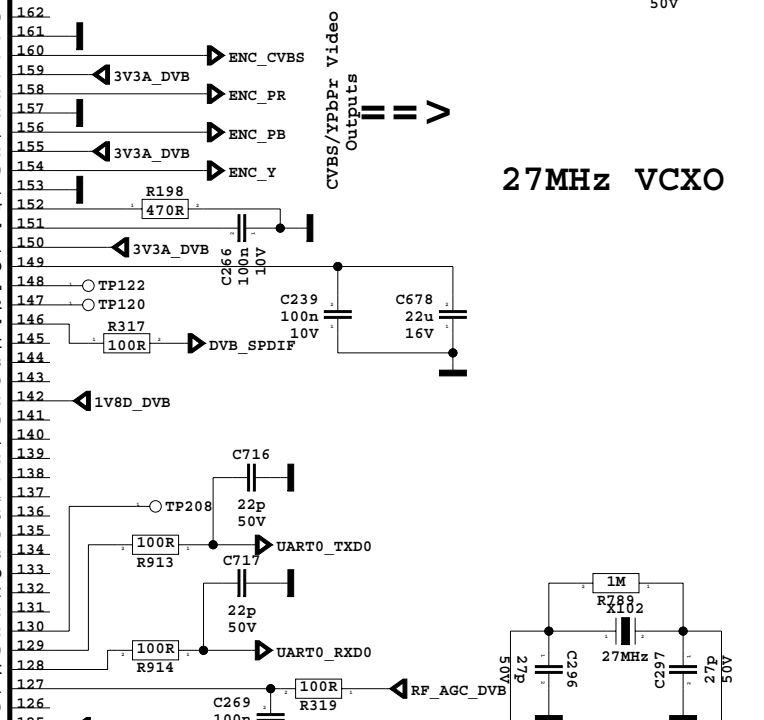
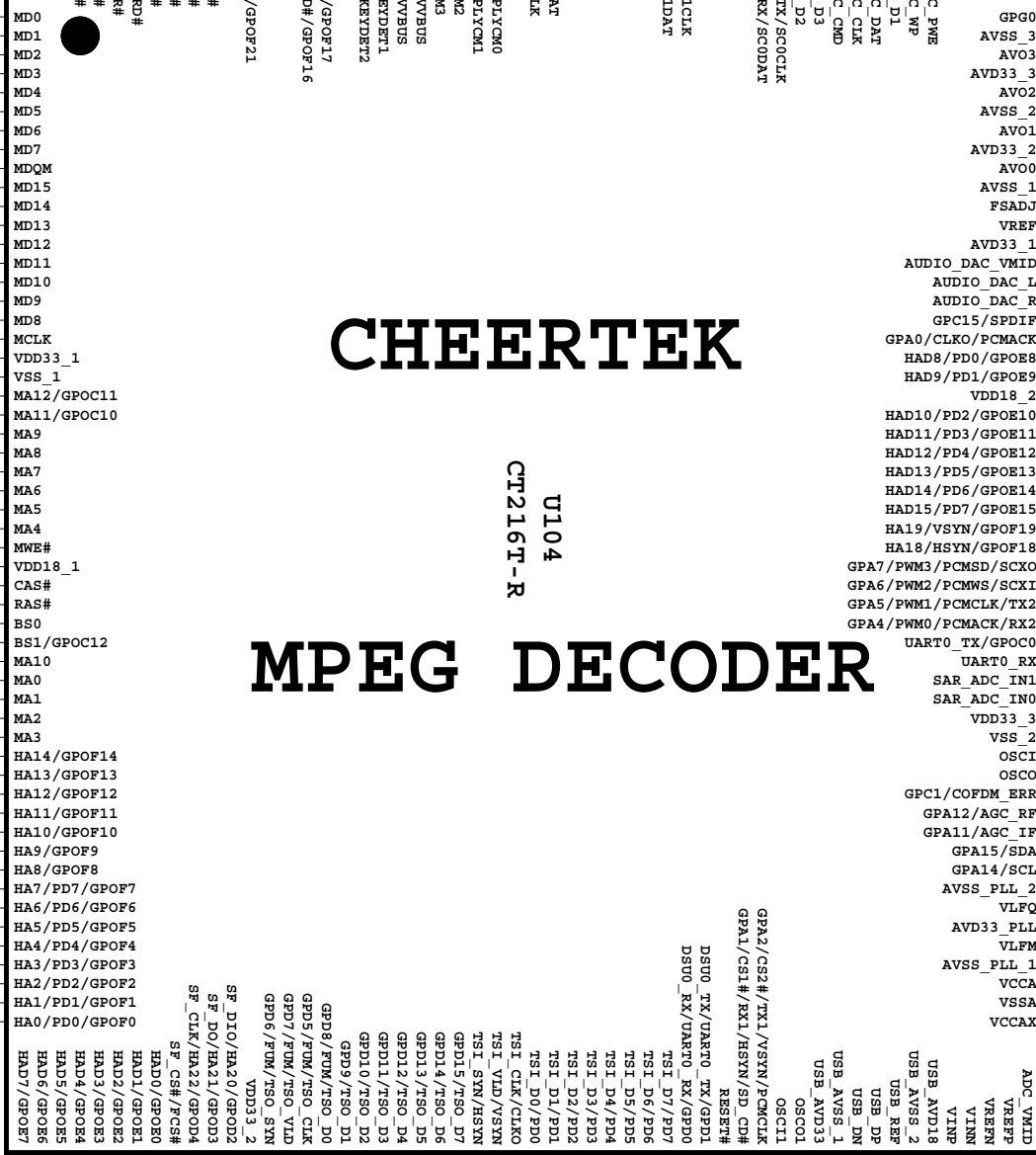
DVB VIDEO FILTER&



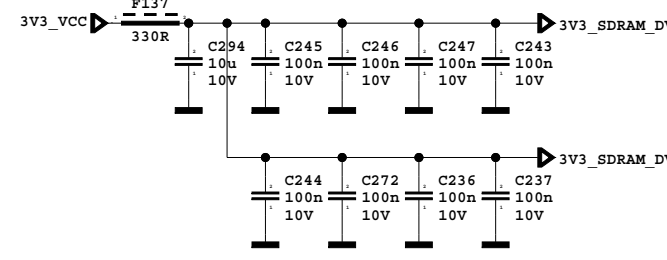
U134 SDRAM



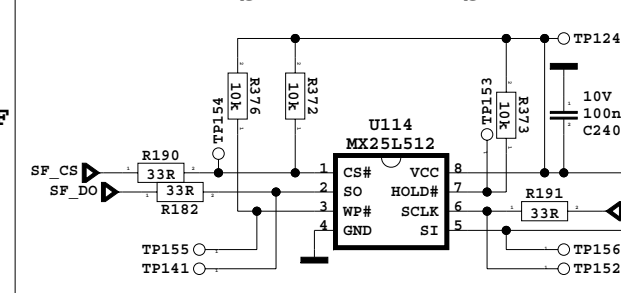
CHEERTEK U104 CT216T-R MPEG DECODER



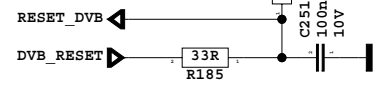
27MHz VCXO



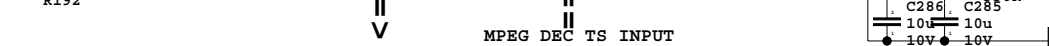
SERIAL FLASH

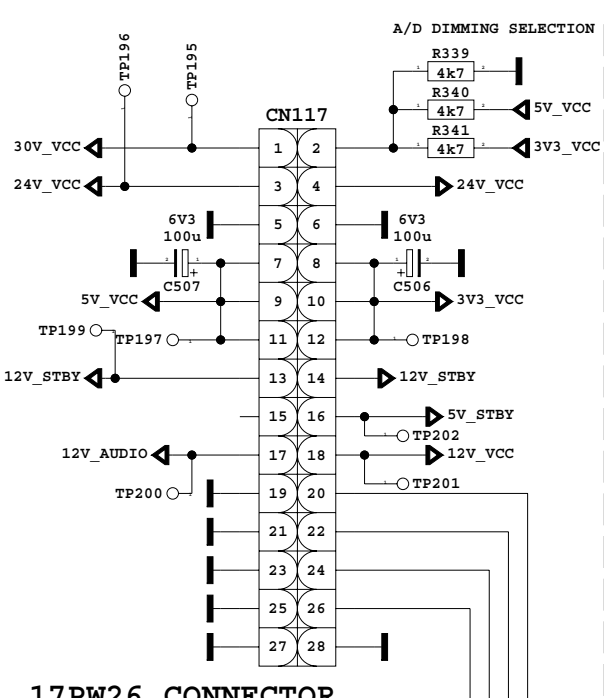


DVB RESET

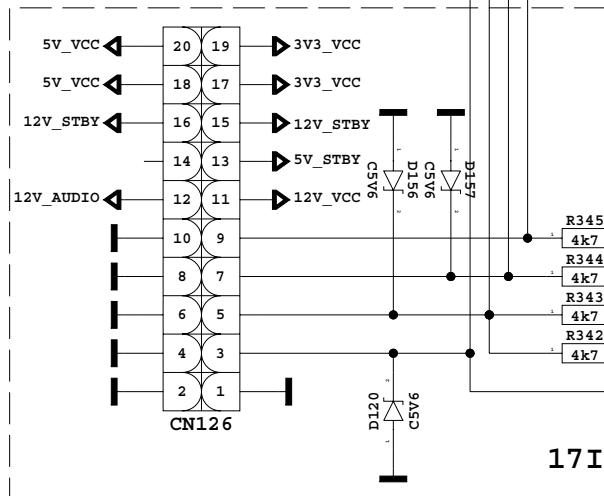


MPEG DEC TS OUTPUT

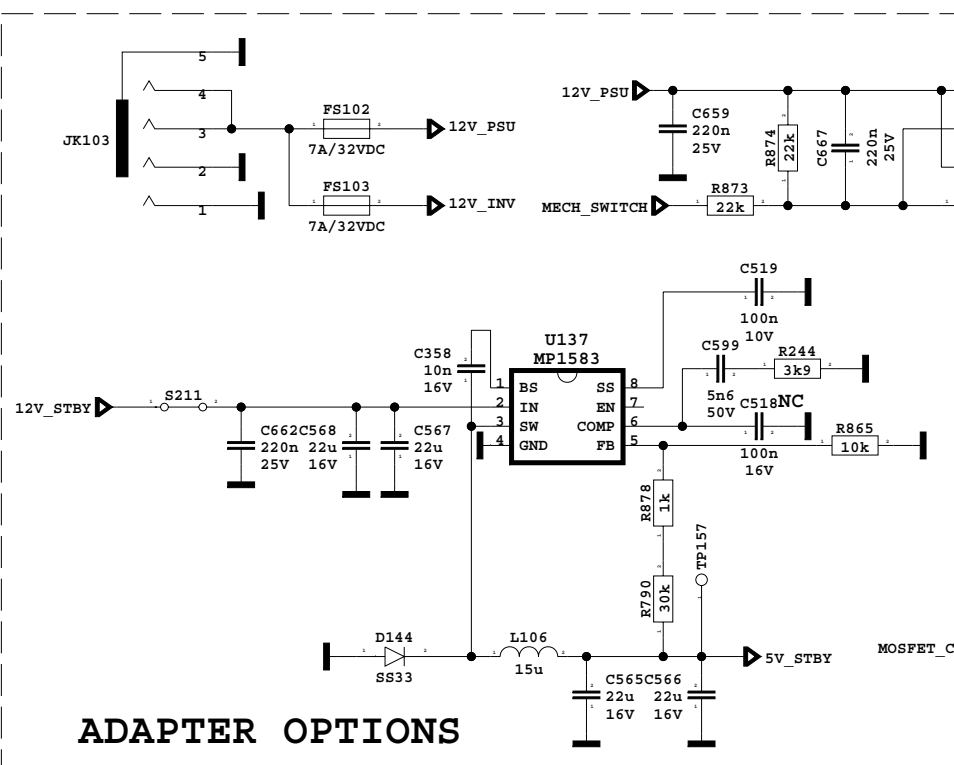




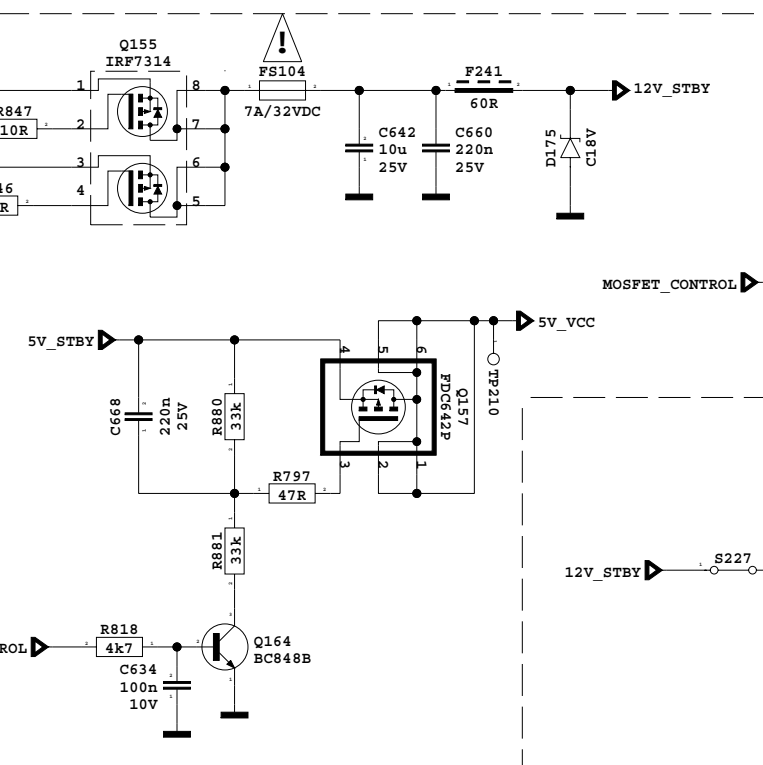
17PW26 CONNECTOR



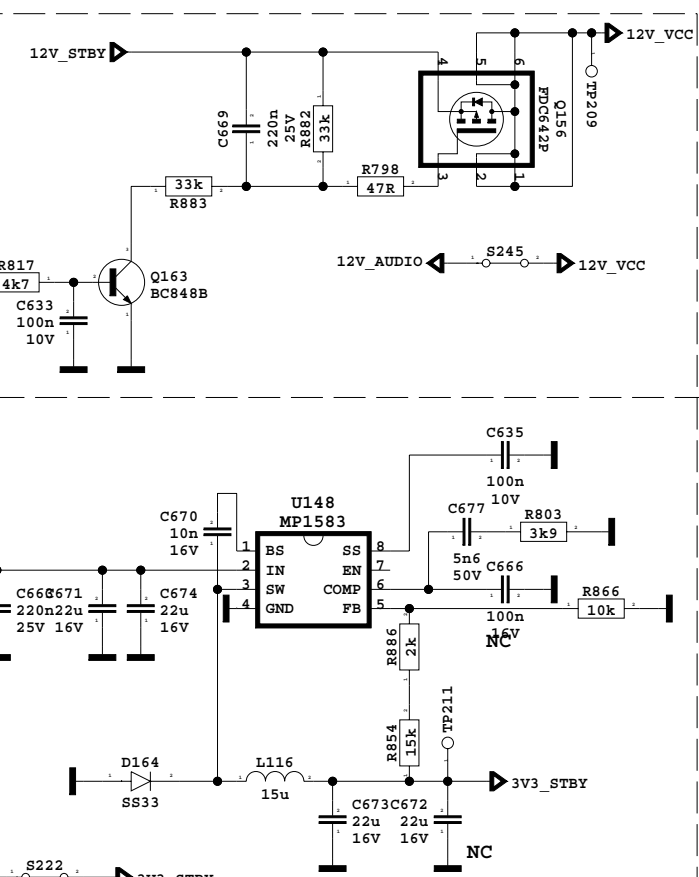
17IPS17 CONNECTOR



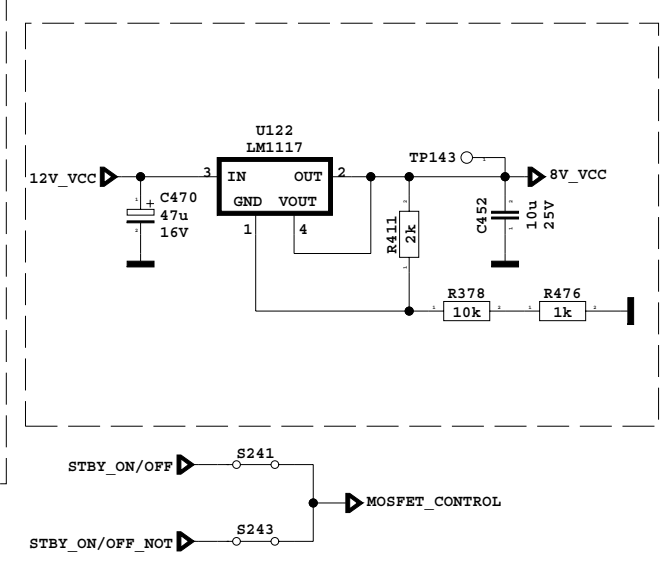
ADAPTER OPTIONS



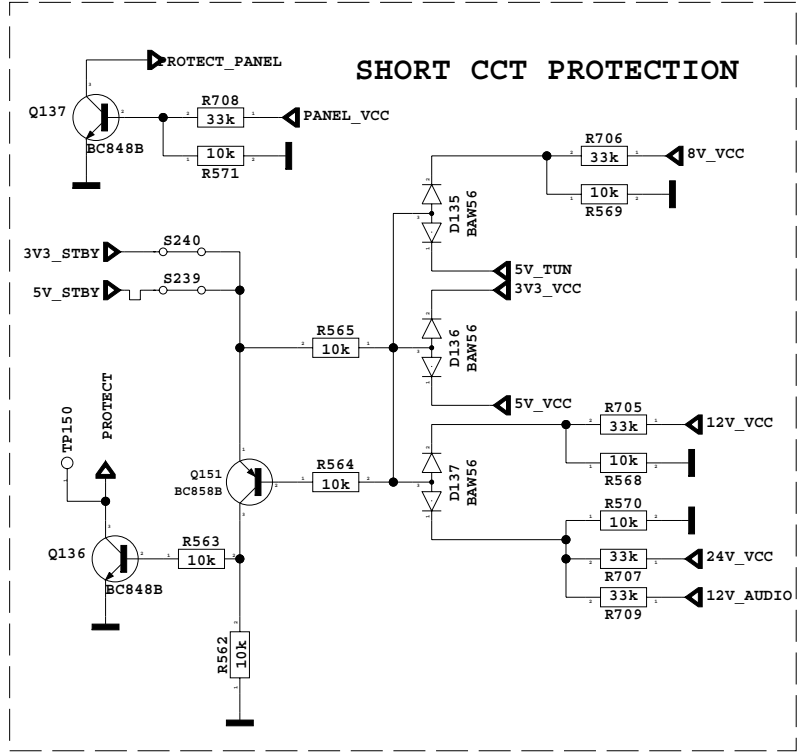
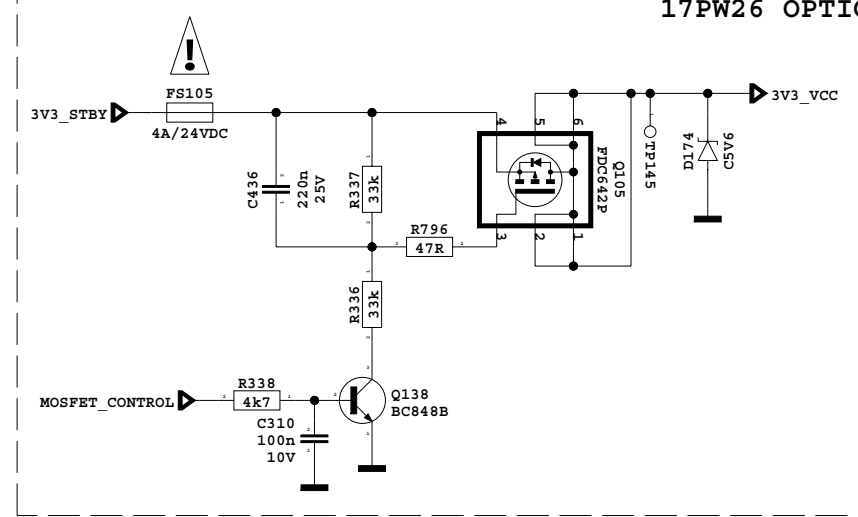
ADAPTER AND IPS15 OPTIONS



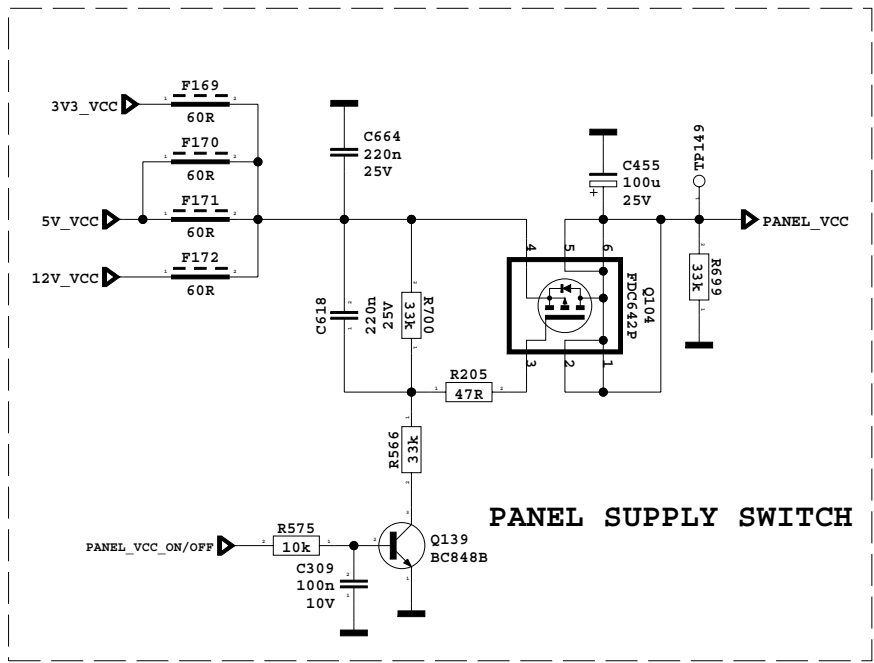
17PW26 OPTIONS



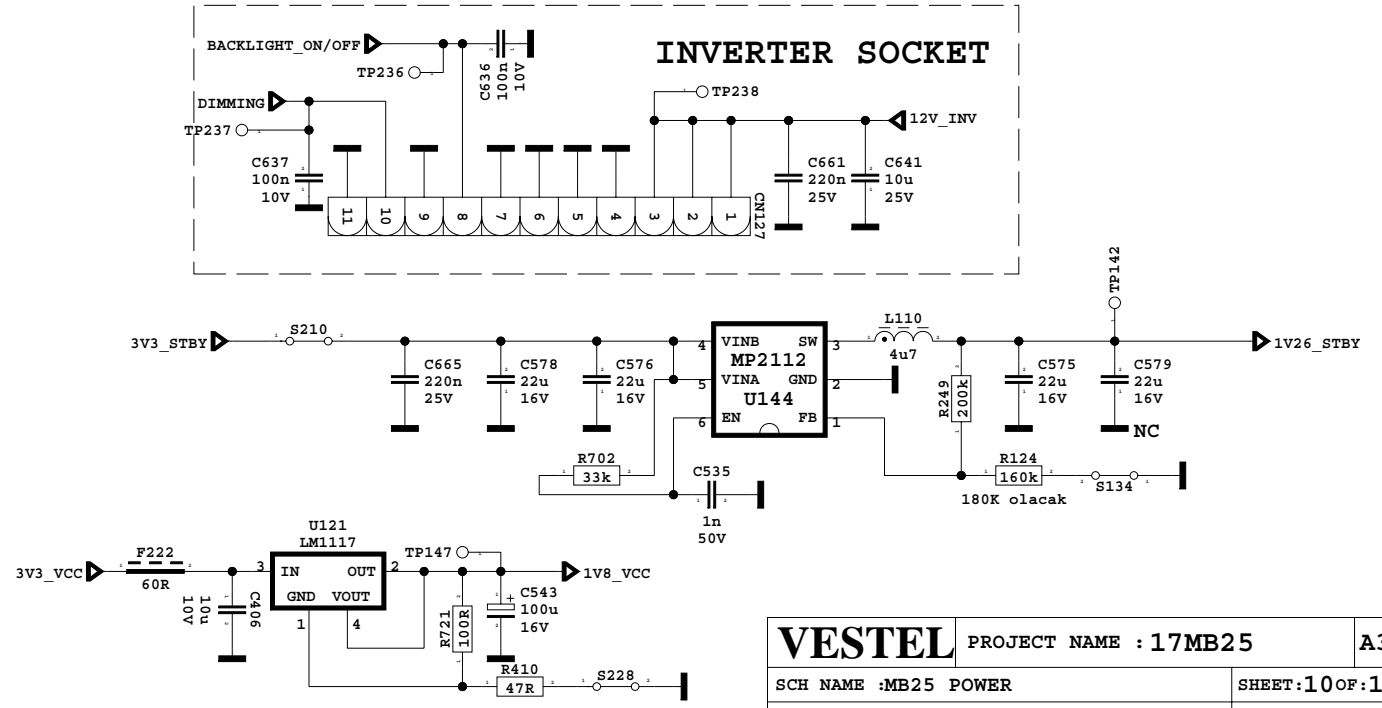
PAULOU DECOUPLING CAPACITORS



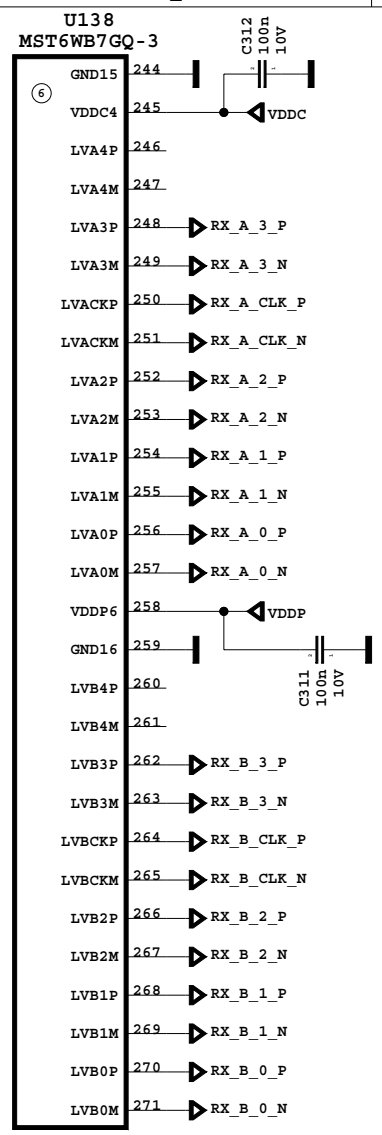
SHORT CCT PROTECTION



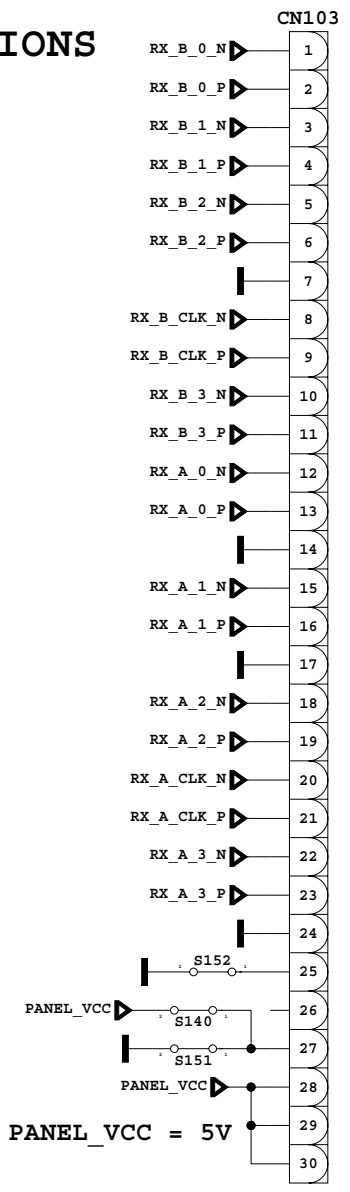
PANEL SUPPLY SWITCH



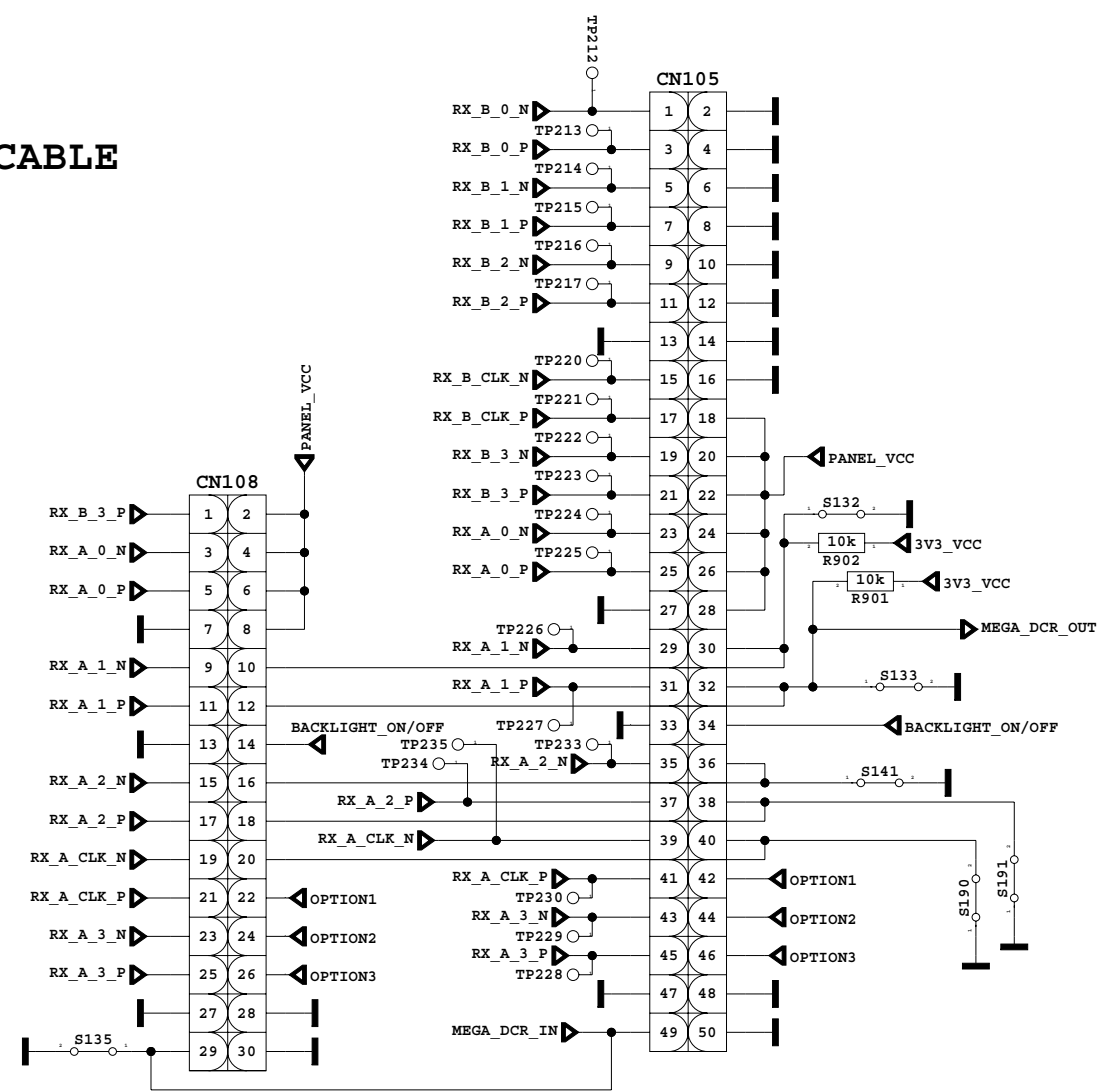
INVERTER SOCKET



19" TO 22" FFC OPTIONS



LVDS CABLE



26" TO 32" FFC OPTIONS

